COMMUNICATION ENGINEERING

GPS AND GALILEO

DUAL RF FRONT-END RECEIVER DESIGN, FABRICATION, AND TEST

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GPS & Galileo: Dual RF Front-end Receiver and Design, Fabrication, and Test

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List of Abbreviations and Acronyms

3G	Third generation of mobile phone standards
A/D	Analog to digital
AC	Alternating current
ADC	Analog-to-digital converter
ADS	Advanced design system
AGC	Automatic gain control
AltBOC	Alternative binary offset carrier
β_0	Low-frequency current gain
BER	Bit error rate
BJT	Bipolar junction transistor
BOC	Binary offset carrier
BPSK	Bi-phase shift key
BW	Bandwidth
C	Capacitance
C/A-code	Coarse acquisition code
C/N_0	Carrier-to-noise ratio (dB)
c/n_0	Carrier-to-noise ratio (expressed as a ratio)
C_{bc}	Base-collector capacitance
C_{BD}	Bulk-drain capacitance
C_{BE}	Base-emitter capacitance
CDMA	Code-division multiple access
CE	Chip enable
CFL	Compact fluorescent lamp
C_{GB}	Gate-bulk capacitance
C_{GD}	Gate-drain capacitance

C_{GS}	Gate-source capacitance
C_L	Load capacitance
C_μ	Base-collector parasitic capacitance
CMOS	Complementary metal-oxide semiconductor
CP	Charge pump
C_π	Base-emitter parasitic capacitance
CPU	Central processing unit
CRT	Cathode ray tube
CS	Commercial service (Galileo)
DC	Direct current
$\Delta\phi$	Phase difference
DGPS	Differential GPS
DGTREN	Directorate-General for Energy and Transport
DNSS	Defense Navigation Satellite System
DoD	Department of Defense
DoT	Department of Transportation
DSP	Digital signal processing
DVD	Digital video disc
EC	European Commission
ECL	Emitter coupled logic
ECP	Extended capability port
EGNOS	European Geostationary Navigation Overlay Service
EPP	Enhanced parallel port
ESA	European Space Agency
ESD	Electrostatic discharge
EU	European Union
FAA	U. S. Federal Aviation Administration
FDD	Floppy disk drive
FDMA	Frequency division multiple access
FEC	Forward error correction
FOC	Full operational system
ϕ_p	Phase margin
F_{ref}	Reference frequency
f_{res}	Resonance frequency
FS	Frequency selection
f_{Xtal}	Crystal frequency
G	Gain

GaAs	Gallium arsenide
GAGAN	Satellite-based augmentation system
Galileo	European GNSS
GC	Gain control
GCA	Gain-controlled amplifier
GDP	Gross domestic product
GIOVE	Galileo in-orbit validation element
GIS	Geographic information system
GLONASS	Russian global navigation satellite system
g_m	Transconductance
G_m	Effective transconductance
$Gmax$	Maximum gain
$Gmin$	Minimum gain
g_{mRF}	Radio frequency transconductance
GMT	Greenwich mean time
GND	Ground
GNSS	Global navigation satellite system
GOC	Galileo operating company
GPS	Global positioning system (U.S. GNSS)
GSM	Global system for mobile communications
GSS	Galileo Sensor Station
G_v	Voltage gain
HA	High accuracy (GLONASS)
HBM	Human body model
HBT	Heterojunction bipolar transistor
HDD	Hard disk drive
I/O	Input/output
I_b	Base current
I_c	Collector current
IC	Integrated circuit
IDE	Integrated drive electronics
I_{DQ}	Bias current of the differential amplifier
I_e	Emitter current
IF	Intermediate frequency
IFA	Intermediate frequency amplifier
IIP3	Input third-order intermodulation product
IP3	Third-order intermodulation product

I_{RF}	Radio frequency current
J/*S*	Jammer-to-signal power ratio
j/*s*	Jammer-to-signal power ratio (expressed as a ratio)
JCAB	Japan's ministry of land, infrastructure and transport
JPO	Joint programme office
JTAG	Joint Test Action Group (IEEE 1149.1 standard)
JU	Joint undertaking
K_{PD}	PFD gain
K_{VCO}	Gain of the voltage-controlled oscillator
L	Transistor length
L_b	Base inductance
LBS	Location-based services
LC	Inductors and capacitors
LCD	Liquid crystal display
L_e	Emitter inductance
Le	Degeneration emitter inductance
LNA	Low-noise amplifier
LO	Local oscillator
LORAN	Long-range radio aid to navigation
LPF	Low pass filter
LPT	Line print terminal
LVDS	Low-voltage differential signaling
MEO	Medium earth orbit
MM	Machine model
MOS	Metal-oxide semiconductor
MP3	MPEG-1 audio layer 3
MPW	Multiproject wafer
MSAS	Multifunctional satellite augmentation system
N	PLL divider division ratio
NASA	National Aeronautics and Space Administration
Navstar GPS	GPS
NF	Noise figure
NMOS	*n*-type channel metal-oxide semiconductor
NUDET	Nuclear detonation detection system
OEM	Original equipment manufacturer
OIP3	Output third-order intermodulation product

OMEGA	Global radio navigation system
OS	Open service (Galileo)
OSD	Office of the Secretary of Defense
P-code	Precision code
PAD	Flat surface in the integrated circuit used to make electrical contact soldering the bonding wire
PC	Personal computer
PCB	Printed circuit board
P_d	Signal detection probability
PDF	Probability density function
P_{fa}	False alarm probability
PFD	Phase frequency detector
P_{in}	Input power
PLL	Phase-locked loop
PMOS	*p*-type channel metal-oxide semiconductor
PN	Phase noise
PN-junction	A junction formed by combining p-type and n-type semiconductors
PNP	Bipolar junction transistor type
P_{out}	Output power
ppm	Parts per million
PPP	Public-private partnerships
PPS	Precise positioning service
PQFP	Plastic quad flat pack
PRN code	Pseudorandom noise code
PRS	Public regulated services (Galileo)
PVT	Position, velocity, and time
Q	Spread spectrum processing gain adjustment factor (dimensionless)
Q	Quality factor
q	Electronic charge
QPSK	Quadrature phase-shift keying
QZSS	Quasi-zenith satellite system
r_b	Base resistance
R_{bias}	Bias resistor
RC	Replacement code
r_c	Collector resistance
R_c	Chipping rate (chips/s)

R_c	Collector resistor
RC-code	Replacement code
r_e	Emitter resistance
R_e	Emitter resistor
RF	Radio frequency
RFIC	Radio frequency integrated circuit
R_L	Load resistance
RLC network	Network composed of at least a resistance, inductance, and capacitance
RMS	Root mean square
ROM	Read-only memory
Rs	Source resistance
S/*N*	Signal-to-noise ratio (dB)
s/*n*	Signal-to-noise ratio (expressed as a ratio)
S11	Input port voltage reflection coefficient
S22	Output port voltage reflection coefficient
SA	Standard accuracy (GLONASS)
SA	Selective availability (GPS)
SAR	Search and rescue
SAW	Surface acoustic wave
SBAS	Satellite-based augmentation system
SiGe	Silicon germanium
σ_n	Root mean square noise power
SNR	Signal-to-noise ratio (dB)
SoL	Safety of life (Galileo)
SOLAS	Safety of life at sea
SPP	Serial port profile
SPS	Standard positioning service (GPS)
SRAM	Static random access memory
SSB	Single-side band
StarFire	Satellite-based augmentation and navigation system
StarFix	DGPS system
System 621B	Satellite navigation system
T	Integration time for every cell before signal detection
T	Temperature
tbd	To be defined
TFT	Thin-film transistor

Timation	Global radio navigation system
TQFP48	48-pin thin quad flat pack
Transit	Satellite navigation system
Tsikada	Satellite navigation system
TTFF	Time to first fix
UMTS	Universal mobile telecommunications system
U.S.	United States
USB	Universal serial bus
UTC	Coordinated universal time
V_{bias}	Bias voltage
VCO	Voltage-controlled oscillator
V_{DD}	Power supply voltage
V_{GS}	Gate-source voltage
VHF	Very high frequency
V_{IF}	Intermediate frequency voltage
V_{in}	Input voltage
V_{LO}	Local oscillator voltage
VNA	Vector network analyzer
v_{nb}	Base-emitter shot noise
v_{nc}	Collector emitter shot noise
v_{nm}	Noise of the mixer converted to a voltage source at the input
v_{nr}	Thermal noise of parasitic resistances
v_{ns}	Noise generated within the source
V_{od}	Differential output voltage
VOR	VHF omnidirectional radio range
V_{RF}	Radio frequency voltage
VSWR	Voltage standing wave ratio
V_t	Threshold voltage
V_T	Thermal voltage
W	Transistor's width
ω_0	Resonance frequency
WAAS	Wide area augmentation system
WAGE	Wide area GPS enhancement
ω_c	Open loop gain bandwidth (third-order filter)
ω_p	Open loop gain bandwidth (second-order filter)
ω_T	Unity gain frequency
Z_{in}	Input impedance

Chapter

1

Introduction

Of the various applications that satellites have been used for, one of the most promising is that of global positioning. Made possible by Global Navigation Satellite Systems, global positioning enables any user to know his or her exact position on Earth. Nowadays, the only fully functioning system is the American Global Positioning System (GPS). However, the European system, known as Galileo, is expected to be operative in 2012.

Since ancient times, mankind has tried to find its bearings by using milestones and stars. A new era has begun, however, thanks to satellite communication. New devices will be necessary to take advantage of both GPS and Galileo systems.

1.1 Satellite Navigation

Navigation is defined as the process of planning, reading, and controlling the movement of a craft or vehicle from one place to another. The word navigate is derived from the Latin root *navis*, meaning "ship," and *agere* meaning "to move" or "to direct." All navigational techniques involve locating the navigator's position by comparing it to known locations or patterns.

Since ancient times, human beings have been developing ingenious ways to navigate. Polynesians and modern navies developed the use of angular measurements of the stars. Everyone engages in some form of navigation in everyday life. When we use our eyes, common sense, and landmarks to find our way when driving to work or walking to a store, we are essentially navigating. Nevertheless, with the development of radios, the need for another class of navigation aids came along. This new phase in navigation called for more accurate information of position,

intended course, and/or transit time to a desired destination. Examples of these navigational aids include a simple clock to determine velocity over a known distance, an odometer to keep track of the distance travelled, and more complex navigation aids that transmit electronic signals such as radio beacons, VHF omnidirectional radio ranges (VORs), long-range radio navigation (LORAN), and OMEGA. With artificial satellites, more precise line-of-sight radio-navigation signals became possible.

The position of anyone with a proper radio-navigation receiver can be computed by means of the signals from one or more radio-navigation aids. In addition to computing the user's position, some radio-navigation aids provide velocity determination and time dissemination. The user's receiver processes these signals, computes its position, and performs the required computational calculations (e.g., range, bearing, estimated time of arrival) so that the user can reach a desired location.

Radio-navigation aids can be classified as either ground-based or space-based. For the most part, the accuracy of ground-based radio-navigation aids is proportional to their operating frequency. Highly accurate systems generally transmit at relatively short wavelengths and the user must remain within the line of sight, whereas systems broadcasting at lower frequencies (longer wavelengths) are not limited to line of sight but are less accurate[Kaplan96], [Parkinson96].

1.1.1 GPS Predecessors

In the early 1960s, several U.S. governmental organizations—including the Department of Defense (DOD), the National Aeronautics and Space Administration (NASA), and the Department of Transportation (DOT)—were interested in developing satellite systems for position determination. The optimum system was viewed as having the following attributes: global coverage, continuous/all weather operation, the ability to serve high-dynamic platforms, and high accuracy.

The system Transit became operational in 1964 and its operation was based on the measurement of the Doppler shift of a tone at 400MHz sent by polar orbiting satellites at altitudes of about 600 nautical miles (ionospheric group delay was corrected by transmitting two frequencies). Transit satellites travelled along well-known paths and broadcasted their signals on a well-known frequency.

The received frequency will differ slightly from the broadcast frequency because of the movement of the satellite with respect to the receiver. If the frequency shift is measured over a short time interval, the receiver can determine its location on one side or the other of the satellite. Many measurements such as these, combined with precise knowledge of the satellite's orbit, can enable a receiver to compute a particular position. This first system had its limitations, as it offered

an intermittent service with limited coverage with periods of 35min. to 100min. of unavailability. However, because of its low velocity, its two-dimensional nature was suitable for shipboard navigation rather than for high dynamic uses, as aircrafts. The technology developed for Transit, which included both satellite prediction algorithms and more than 15 years of space system reliability, exceeding expectations more than two or three times, has proved to be extremely useful for GPS. Limitations of early developed spaced-based systems (the U.S. Transit and the Russian Tsikada system) led to the development of both the U.S. Global Positioning System (GPS) and the Russian Global Navigation Satellite System (GLONASS).

Overcoming these early systems' shortcomings required either an enhancement of Transit or the development of another satellite navigation system with the desired capabilities previously mentioned. By 1972, breakthroughs were made by installing high-precision clocks in satellites. These satellites, known as Timation, were used principally to provide highly precise time and time transfer between various points on Earth. They additionally provided navigational information. Several variants of the original Transit system were proposed, among them the inclusion of highly stable space-based atomic clocks in order to achieve precise time transfer. Modifications were made to Timation satellites to provide a ranging capability for two-dimensional position determination, employing side-tone modulation for satellite-to-user ranging.

Later models of the Timation satellites employed the first atomic frequency standards (rubidium and cesium), which typically had a frequency stability of several parts per 10^{12} (per day) or better. This frequency stability greatly improves the prediction of satellite orbits (ephemerides) and also lengthens the required update time between control segment and satellites. This revolutionary work in space-qualified time standards was also important for the development of GPS.

At the same time as the Navy was considering the Transit enhancements and undertaking the Timation efforts, the Air Force conceptualized a satellite positioning system denoted as System 621B. By 1972, this programme had already demonstrated the operation of a new type of satellite-ranging signal based on pseudorandom noise (PRN). The signal modulation was essentially a repeated signal sequence of fairly random bits (ones or zeros) that possessed certain useful properties. The start ("phase") of the repeated sequence could be detected and used to determine the range of a satellite. The signals could be detected even when their power density was less than $1/100^{th}$ that of ambient noise and all satellites could broadcast on the same nominal frequency because properly selected PRN codes were nearly orthogonal. The ability to reject noise also implied a powerful ability to resist most forms of jamming or deliberate interference.

The use of pseudorandom noise (PRN) modulation for ranging with digital signals provided three-dimensional coverage and continuous worldwide service. The use of PRN modulation with ranging (i.e., pseudoranging), which could be considered the third foundation of the GPS system, was developed through Army research.

In 1969, the Office of the Secretary of Defense (OSD) established the Defense Navigation Satellite System (DNSS) programme to consolidate the independent development efforts of each military branch into a single joint-use system. The OSD also established the Navigation Satellite Executive Steering Group, which was put in charge of determining the viability of a DNSS and planning its development. This endeavour led to the forming of the GPS Joint Programme Office (JPO) in 1973, which set the development of Navstar GPS in motion. This was not exclusively the concept of any prior system but rather was a synthesis of them all. The JPO's multibranch approach avoided any basis for further bickering because all contending parties were part of the conception process. From that point on, the JPO acted as a multiservice enterprise, with officers from all branches attending meetings that were previously exclusive. The system is generally referred to as simply GPS.

In 1973, the first phase of the programme was approved. It included four satellites (one was a refurbished test model), launch vehicles, three varieties of user equipment, a satellite control facility, and an extensive test programme. The first satellite prototype was launched in 1978. By this time, the initial control segment was deployed and working and five types of user equipment were undergoing preliminary testing.

More than four satellites were now required. The minimum number of satellites required to determine three-dimensional position is four. Any launch or operational failure would have gravely impacted the first phase of GPS testing. The problem of the need for spare satellites was solved by joining the Transit programme, which was followed by the development of two additional satellites. Apart from extending GPS, this joint endeavour avoided the possibility of having two systems competing against each other.

Even though today's GPS system concept is the same as the one proposed in 1973, its satellites have expanded their functionality to support additional capabilities. Although the orbits are slightly modified, the original equipment designed to work with the very first four satellites would still work today[Kaplan96], [Parkinson96].

1.1.2 Galileo

The European Union (EU) and European Space Agency (ESA) agreed on March 2002 to introduce an alternative to GPS, called the Galileo positioning system. The system is scheduled to be working in 2012.

The first experimental satellite was launched on December 28, 2005. Galileo is expected to be compatible with the modernized GPS system. The receivers will be able to combine the signals from both Galileo and GPS satellites to increase accuracy significantly.

In 1999, the European Commission presented its plans for a European satellite navigation system defined by a joint team of engineers from Germany, France, Italy, and the United Kingdom. Contrary to its American and Russian counterparts, Galileo is designed specifically for civilian and commercial purposes. The United States reserves the right to limit the signal strength or accuracy of the GPS systems or to shut down public GPS access completely (although it has never done the latter) so that only the U.S. military and its allies would be able to use it in time of conflict. Until 2000, the precision of the signal available to non–U.S. -military users was limited, due to a timing pulse distortion process known as selective availability. The European system will be subject to shutdown only for military purposes under extreme circumstances (although it may still be jammed by anyone with the right equipment). Both civil and military users will have complete and equal access to this system.

The European Commission faced certain challenges in finding funding for the project's subsequent stage, because of national budget constraints across Europe. The United States government opposed the project, arguing that it would jeopardize the ability of the United States to shut down GPS in times of military operations in the wake of the September 11, 2001, attacks. In 2002, as a result of U.S. pressure and economic difficulties, the Galileo project was almost put on hold. However, a few months later, the situation changed dramatically. Partially in reaction to the pressure of the U.S. government, European Union member states decided it was important to have their own independent satellite-based positioning and timing infrastructure.

The European Union and the European Space Agency agreed in 2002 to fund the project. The first stage of the Galileo programme was agreed upon officially in 2003 by the EU and the ESA. The plan was for private companies and investors to invest at least two-thirds of start-up costs, with the EU and ESA dividing the remaining cost. An encrypted higher-bandwidth Commercial Service with improved accuracy would be available at extra cost, with the base Open Service freely available to anyone with a Galileo-compatible receiver.

In 2007, it was agreed to reallocate funds from the EU's agriculture and administration budgets and to soften the tendering process in order to woo more EU companies to join the project. In 2008, EU transport ministers approved the Galileo Implementation Regulation, which freed up funding from the EU's agriculture and administration budgets.

This allowed the issuing of contracts to start construction of the ground station and satellites.

From its conception, a fundamental part of the Galileo programme was to be a worldwide system that would maximise its benefits by means of international cooperation. Such cooperation is foreseen to help to reinforce industrial know-how and to minimise the technological and political risks involved. This includes, quite naturally, cooperation with the two countries now operating satellite navigation systems. Europe is already examining a number of technical issues with the United States related to interoperability and compatibility with the GPS system. The objective is to ensure that everyone will be able to use both GPS and Galileo signals with a single receiver. Negotiations with the Russian Federation, which has valuable experience in the development and operation of its GLONASS system, are also ongoing.

In addition to the technical harmonisation required among Galileo and existing satellite navigation systems, international cooperation is necessary in the development of ground-based equipment and ultimately to promote widespread use of this technology. Such cooperation also falls in line with the objectives of the European Union with respect to foreign policy, co-operation with developing countries, employment, and the environment. Several non-European countries have already contributed to the Galileo programme in terms of system definition, research, and industrial cooperation. Since the European Council's decision to launch the Galileo programme, even more countries have expressed the wish to be associated with the programme in one form or another. Indeed, the European Commission sees Galileo as highly relevant to all the countries of the world and remains committed to further collaboration with countries that share its vision of a high-performance, reliable, and secure global civil satellite navigation system. In 2003, China joined the Galileo project and invested heavily in the project over the following few years. In 2004, Israel signed an agreement with the EU to become a partner in the Galileo project. In 2005, the Ukraine, India, Morocco, and Saudi Arabia signed an agreement to take part in the project. At the time of publication, the most recently added member to the project was South Korea, which joined the programme in 2006.

In 2007, the 27 member states of the European Union collectively agreed to move forward with the project, with plans for bases in Germany and Italy[EU-Galileo].

Two Galileo System Test Bed satellites, dedicated to take the first step of the In-Orbit Validation phase towards full deployment of Galileo, can be found under the name of GIOVE, which stands for Galileo In-Orbit Validation Element. At the time of publication, the following milestones had been accomplished:

- In 2005, GIOVE-A, the first GIOVE test satellite, was launched.
- In 2008, GIOVE-B, with a more advanced payload than GIOVE-A, was successfully launched.
- In 2008, the GIOVE-A2 satellite was ready to be launched.

1.1.3 Satellite Based Augmentation System (SBAS)

A Satellite Based Augmentation System (SBAS) is a system that supports wide-area or regional augmentation by using additional information sent by these satellites. In addition to the satellites, such systems are also composed of well-known multiple ground stations that take measurements of one or more of the Global Navigation Satellite System (GNSS) satellites, their signals, or other environmental factors that may influence the signal received by users. SBAS information messages are created from these measurements and sent to one or more satellites to be transmitted to users.

Therefore, Satellite Based Augmentation Systems use external information within the user's receiver to improve the accuracy, reliability, and availability of the satellite navigation signal of a GNSS. There are many such systems in place that are generally named depending on the way that the external information reaches the receiver. Such information includes additional information about sources of error (such as clock drift, ephemeris, or ionospheric delay), direct measurements of how much the signal was off in the past, or additional vehicle information to be integrated in the calculation process.

Examples of augmentation systems of various SBAS are as follows. Note that the last two are commercial systems.

- The Wide Area Augmentation System (WAAS), operated by the United States Federal Aviation Administration (FAA)
- The European Geostationary Navigation Overlay Service (EGNOS), operated by the European Space Agency
- The Wide Area GPS Enhancement (WAGE), operated by the United States Department of Defense for use by military and authorized receivers
- The Multifunctional Satellite Augmentation System (MSAS) system, operated by Japan's Ministry of Land, Infrastructure and Transport (JCAB)
- The Quasi-Zenith Satellite System (QZSS), proposed by Japan
- The GAGAN system, proposed by India

- The StarFire navigation system, operated by John Deere
- The Starfix DGPS System, operated by Fugro

1.2 Positioning through Satellites

A GNSS calculates the location of fixed and moving objects anywhere in the world by means of precise timing and geometric triangulation (see Figure 1-1). GNSS is composed of a constellation of satellites that send radio signals.

A combination of personalised radio signals, which are encoded with the precise time they left the satellite, allows a ground receiver to determine its position through geometrical triangulation (Figure 1-1). Satellites are equipped with high-precision atomic clocks enabling them to measure time accurately. Receivers hold information regarding the position of any satellite at any given time. Thus, a precise position can be calculated by timing how long the signals take to reach the receiver from the satellites in view. By reading the incoming signal, the receiver can recognise a particular satellite, determine the time taken by the

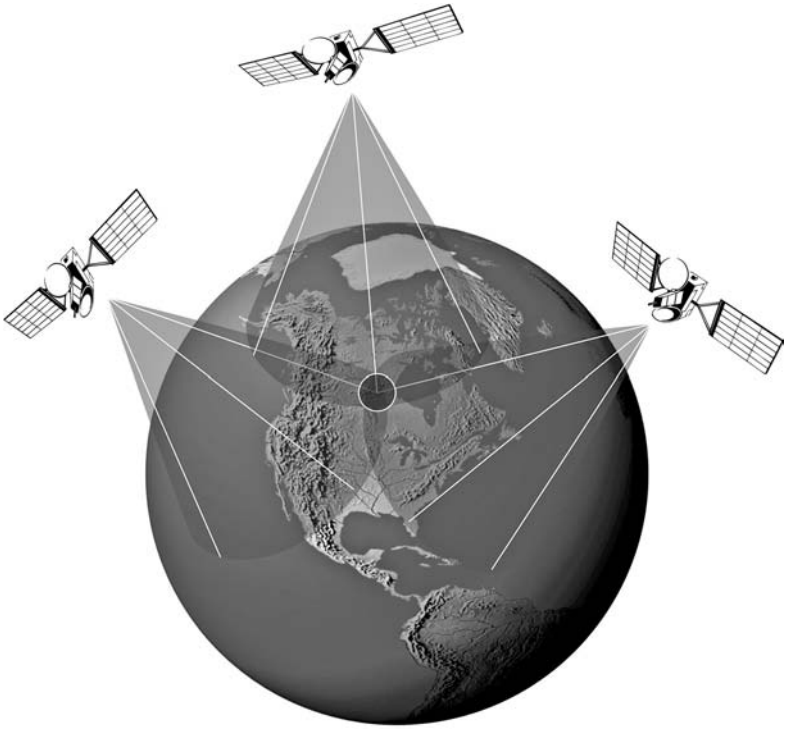

Figure 1-1 Satellite triangulation for positioning

signal to arrive, and therefore calculate the distance between itself and the orbiting satellite.

A ground receiver should theoretically be able to calculate its three-dimensional position (latitude, longitude, and altitude) by triangulating the data from three satellites simultaneously. However, a fourth satellite is necessary to address a "timing offset" that occurs between the clock in a receiver and those in satellites. The more satellites there are, the greater the accuracy is. As satellites are synchronised with Coordinated Universal Time (UTC), they provide precise time.

Functioning around the clock, GNSS satellites provide accurate three-dimensional positioning to anyone with appropriate radio reception and processing equipment. Although the coverage provided by a GNSS is "global," its availability and precision varies according to local conditions. Signals tend to be weaker over the poles and in low-lying urban areas surrounded by buildings.

1.2.1 GNSS Systems

Nowadays, there are only two systems that provide global coverage: the U.S. Navstar GPS and the Russian GLONASS. Although the American system is fully operational, the Russian programme is only partially available due to the decaying constellation of its satellites, owing in part to financial constraints stemming from the collapse of the Soviet Union. Both systems began as military applications and continue to be funded and operated by their respective departments of defence. Nevertheless, both systems were made available to the civil population, although they remain under total military control and are less precise than the original systems. The European Galileo is set to become the third GNSS provider, as it is planned to be operational in 2012. Galileo will offer total interoperability with GPS and GLONASS. The spectrum for the three systems is shown in Figure 1-2.

The current GPS system is based on 24 satellites circling the earth every 12 hours, located in six orbital planes at a height of 20200km (see Figure 1-3). Each satellite sends UTC and navigation data using the

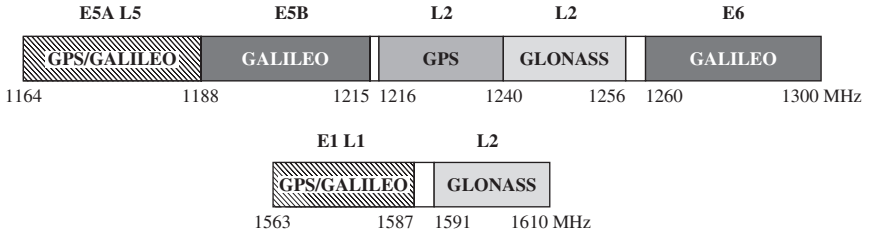

Figure 1-2 GNSS spectrum, GPS, Galileo, and GLONASS

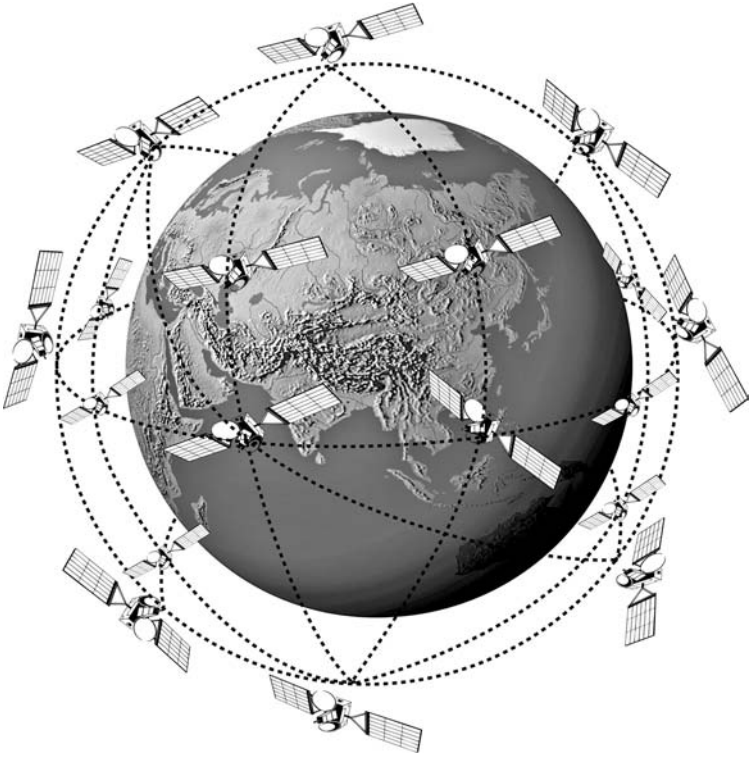

Figure 1-3 Satellite constellation

spread spectrum code-division multiple access (CDMA) technique. A receiver can calculate its own position and speed by correlating the signal delays from any four satellites and combining the result with orbit-correction data sent by the satellites. Currently, two services are provided by GPS: a precise positioning service (P-code), which is mainly restricted to military use; and a standard positioning service (C/A-code), which is less precise than the P-code but available to the public. All 24 satellites transmit signal L1, which carries the C/A-code and the P-code, and signal L2, which carries the P-code. The characteristics of the L1 and L2 signals are shown in Table 1-1. Interference between signals of different satellites

TABLE 1-1 GPS signal characteristics

Signal	Modulation	Central frequency	Bandwidth
L1	QPSK	1575.42MHz	~20MHz (C/A Code 2MHz + P-Code 20MHz)
L2	BPSK or QPSK	1227.6MHz	~20MHz (P-Code 20MHz or P-Code + C/A Code)

TABLE 1-2 GLONASS signal characteristics

Signal	Modulation	Frequency
L1	BPSK	1602MHz + n0.5625MHz
L2	BPSK	1246MHz + n0.4375MHz

is avoided by using pseudorandom signals with low cross-correlation for code division multiple access (CDMA) modulation[ARINC06].

The GLONASS system, like the GPS, consists of 24 satellites placed in three orbital planes at 19100km. Each satellite orbits the Earth approximately every 11 hours and 15 minutes. Two services are offered: standard accuracy (SA), designed to be used by civilians worldwide; and high accuracy (HA), used only by authorisation of the Russian Ministry of Defence. Both signals sent by GLONASS, the characteristics of which are summarized in Table 1-2 [GLONASS02], have frequency division multiple access (FDMA) technology in the L-band for both SA L1 and HA L2.

Similarly, the Galileo system will consist of 30 satellites (27 operational, 3 in reserve), positioned in three circular Medium Earth Orbit (MEO) planes at 23616km above the Earth and inclined at 56° to the equator for planet coverage. As in the GPS system, a receiver will be able to calculate its own position and speed by correlating the signal delays from any four Galileo satellites and combine the result with orbit correction data sent by satellites. Four services will be provided by Galileo: Open Service (OS) (available to everyone); Safety of Life (SoL), Commercial (CS) and Public Regulated (PRS). All these services will be provided by a complex signal structure, which includes as many as 10 signal components. The E1 and E5A-B signals are designated for Open Service. Their characteristics are summarised in Table 1-3[Guenter02].

The GNSS architecture typically consists of three subsystems: a satellite constellation (space segment), a ground segment (control and monitoring ground stations), and end-user mobile receivers. These subsystems can be enhanced through space- or ground-based augmentation [HP AN1272].

1.2.2 Commercial Applications

Over the last few years, the United States and the European Union have been in a race to launch new versions of GNSS, GPS, and Galileo. For the United States, it will be its second generation of GPS, as U.S. Commerce Department secretary announced last January, “the second generation

TABLE 1-3 Galileo signal characteristics

Signal	Modulation	Central frequency	Bandwidth
E1	BOC(1,1)	1575.42MHz	~24MHz
E5A-B	Alt-BOC(15,10)	1191.795MHz	~51MHz

has been born with a commercial focus as it has a second channel for civilian use." This means an increase in accuracy and reliability. Some companies such as General Motors, IBM, Lucent Technologies, and Trimble Navigation have already shown interest. On the other hand, the EU, as well as its partners such as China and India, among others, is involved in the launching of Galileo. In December 2005, the first Galileo satellite, Giove-A, was put into orbit from the Baikonur Cosmodrome in Kazakhstan. At the same time, another important achievement was made when ESA, Europe, and their partners signed an agreement, pledging €950 million to carry out the second phase of the system. This phase consists of the validation of the project, the addition of four satellites, and the establishment of the Galileo ground network. The third phase, which will see the rest of the Galileo satellites put into orbit, is expected to cost around €3.6 billion.

To understand the interest behind those millionaire investments, we need to take a harder look at the possibilities offered by GNSS.

1.2.2.1 GNSS Applications Apart from military applications, GNSS offers a multitude of commercial opportunities. The growth of the transport sector, the skyrocketing evolution of telecommunications, and the development of services requiring precise positioning capabilities – such as rescue services – reinforce the promise of GNSS as an invaluable multiple-use technology (see Figure 1-4).

Signal transmissions are an integral component of aviation, shipping, telecommunications, and computer networks, to name just a few applications in which they are used. Positioning plays an important role in these fields due to its ability to enhance economic efficiency. For example, in aviation, savings may be obtained through more direct flights (attained through improved traffic management), more efficient ground control, improved use of airspace capacity, and fewer flight delays. GPS is already an important tool for in-flight safety, assisting in such aspects as en route navigation, airport approach, landing, and ground guidance. It is estimated that Galileo's economic benefits to European aviation and shipping sectors will reach €15 billion in 2020[EU-Galileo].

Many industries will benefit from advantages offered by GNSS, such as defence, aeronautics, and mining. Similar effects on the mass market, motor vehicles, and surveying will be explained in detail in the following section.

1.2.2.1.1 Mass Market People are starting to discover the realm of recreational possibilities offered by GNSS. Experts predict that more than 40 million potential users in Europe will use GNSS for recreational purposes such as sport fishing, sea navigation, and hiking. As with any mass market, demand elasticity is a key factor, as is price. Nowadays a

Figure 1-4 Applications for GNSS

basic receiver costs around €100, yet consumers will soon demand retail prices of less than half that cost. GNSS manufacturers, therefore, have no choice but to decrease receiver cost and size.

On the other hand, mandatory services such as the European E112 and American E911 will force telephone providers to pinpoint the location of their users from any call down to a 100m radius. Thus, mobile phones will have to include a GNSS receiver. Taking into account the 860 million users of mobile telephones in September 2002 and the prediction of over 2 billion users by 2020, sales for GNSS mobile phone receivers alone will be huge. The U.S. market is currently gearing up for this change thanks to companies such as Qualcomm or Motorola, which are offering GPS-equipped mobile phones.

GNSS will also prove to be an invaluable medical and social tool when it comes to locating Alzheimer's patients and the blind, among others. Moreover, GNSS already plays an important role in emergency services such as search and rescue, disaster relief and environmental monitoring. Current emergency beacons operate within the Cospas-Sarsat satellite system. However, with no real-time service guarantees and inaccurate estimates (provided in kilometres), there is room for improvement.

1.2.2.1.2 Motor Vehicles The motor vehicle market is continuously expanding. It is estimated that more than 670 million cars, 33 million buses and trucks, and more than 200 million motorbikes and light vehicles will be on the streets by 2010. Moreover, by 2020 at least 450 million vehicles will be fitted with GNSS. Thanks to their low cost, GNSS devices will become standard features even in mid-to-low-priced cars. Furthermore, most of the installed devices will be dual systems that work with GPS and Galileo simultaneously. This will increase receiver accuracy and introduce new features, including collision prevention, emergency service notification of airbag activation, or the location of stolen vehicles. This market is expected to be worth €25 billion by 2016.

On the other hand, according to DGTREN, the social and economic costs of road accidents and fatalities amount to 1.5 to 2.5 percent of the European Gross Domestic Product (GDP). Road congestion adds additional costs equivalent to 2 percent of European GDP. The use of high-precision GNSS devices could lower these social costs by increasing road safety, reducing travel time, and minimising road congestion. More efficient use of fuels may also have positive effects on the environment. Additional road applications presently gaining attention include in-car navigation, fleet management of taxis, and driver assistance.

1.2.2.1.3 Surveying A huge increase in surveying-based applications is expected, namely in the trucking and shipping industries, especially if the price for surveying systems drops. This can be achieved by reducing the cost of system electronics.

1.2.2.2 Sales Estimates Sales estimates for upcoming years have been thoroughly studied by market survey consultants in[DGTREN03]. Figure 1-5 shows the expected profits generated by GNSS hardware over the next few years, and Figure 1-6 shows annual earnings in the navigation and

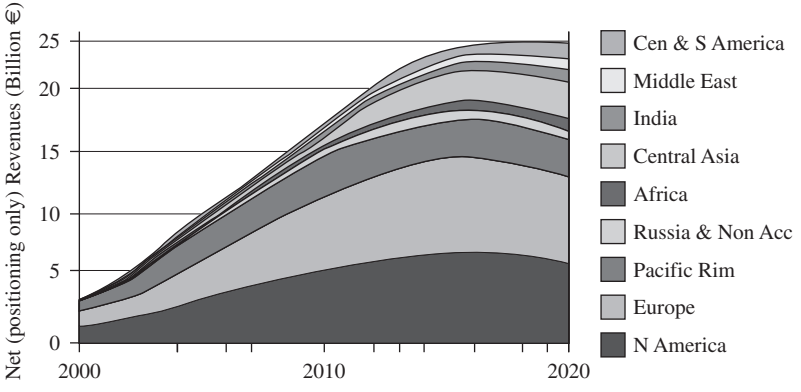

Figure 1-5 GNSS hardware profits [DGTREN03]

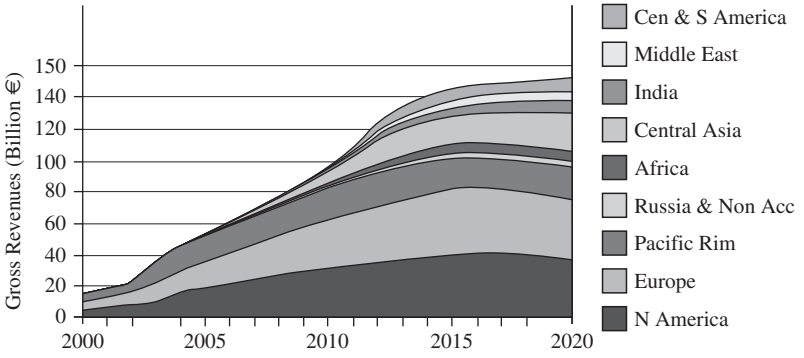

Figure 1-6 Navigation and location system market profits [DGTREN03]

location system market, including hardware. The growth in the next decade of GNSS-related markets can be seen. It presents a great opportunity for those able to offer technological solutions to market needs.

Figure 1-7 shows which industries made up the GNSS business market in 2001 and the market forecast for 2015. The consumer and motor vehicle markets will see the highest growth. The former went from being almost nonexistent to very significant. Location and surveying markets will experience more steady growth than the first two.

GNSS systems will undoubtedly play an important role in the world economy, specifically in regard to services offered and products sold (see Figure 1-8), intensifying the interest of Europe and its partners in having their own system.

1.2.3 System Limitations and Vulnerabilities

Despite military and commercial advantages, GNSS has its limitations. There are three frequently documented weaknesses. First, positioning

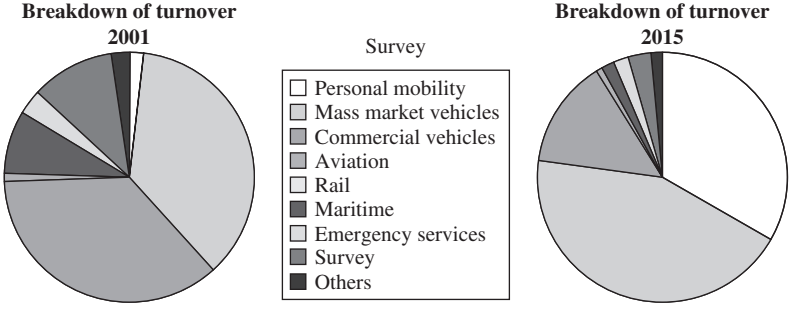

Figure 1-7 Market share for GNSS applications [DGTREN03]

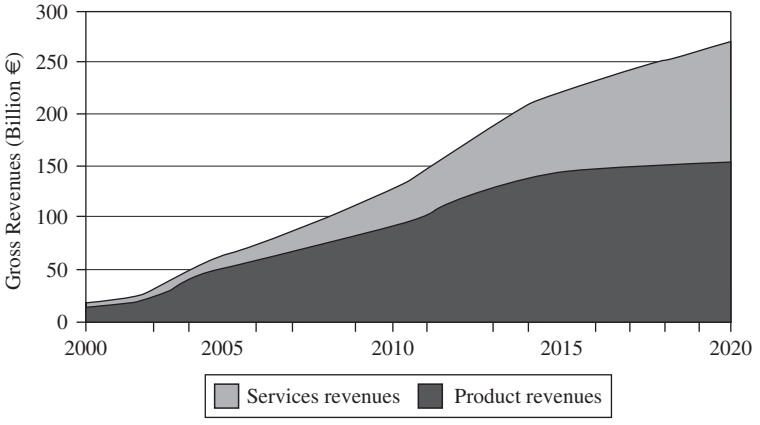

Figure 1-8 Market share for GNSS applications [DGTREN03]

signals tend to be less precise in urban environments or under foliage, in areas where the number of satellites in sight are low (typically at upper and lower latitudes around the poles) and under certain weather conditions such as thick clouds. Transmission strength also affects GNSS precision. A more powerful and less distorted signal could increase precision significantly. To address this, ground or space-based augmentation such as additional ground stations can be used to improve precision in localised areas.

In addition, GNSS services may suffer from intermittent service coverage. Given the limited lifespan of the space component, the system needs to be replaced and/or reconfigured periodically. For example, during certain upgrading operations, receivers relying on information from ground stations or satellites under maintenance may be affected. Even if service suffers setbacks of only a couple of seconds or minutes, the impact may be significant for many applications, such as air traffic control.

Finally, as a vital component for a growing number of commercial and military applications, global navigation and positioning systems may be vulnerable to hostile parties. For example, a ground station may be physically attacked or taken over, resulting in any number of consequences to service, or parts of the system can be electronically jammed. In the distant future, these threats may also affect the space sector, resulting in potentially severe consequences.

The greater the dependence on the system is, the more serious the economic consequences of system failure or shutdown could be. In addition, any system failure could prove to have direct consequences on sectors (such as aviation) requiring continual and precise signals[ISS02], [EU-Galileo].

1.2.4 Dual Receivers, Overcoming Limitations

To provide enhanced services, receivers will have to be able to obtain specific information through signals sent by satellites of both GPS and Galileo systems.

To meet this need, highly integrated low-cost GPS/Galileo receivers will be required. The interoperability of both systems will offer a number of very important advantages. Moreover, to ensure low price and reliability, developers will design receivers with the lowest possible number of external components, low power consumption, and smaller size, and use low-cost technology to fabricate the devices.

1.2.4.1 Why a GPS/Galileo Receiver? As the majority of satellite navigation applications are currently based on GPS, great technological effort is being spent to integrate satellite-derived information with a number of other techniques in order to obtain better positioning precision with improved reliability.

This scenario will significantly change in the near future since the GNSS infrastructure will double in size with the introduction of Galileo. The availability of two or more constellations, more than doubling the total number of available satellites in the sky, will enhance service quality, increasing the number of potential users and applications.

Galileo-specific characteristics will include significant enhancements. First, for urban areas or indoor applications, the design of Galileo signals will improve service availability by broadcasting dataless ranging channels, in addition to the classical pseudorandom ranging codes. Second, the high-end professional market will also benefit from the characteristics of Galileo signals, which will lead to centimetre-sensitive accuracy over large regions[EU-Galileo].

A comparison between Galileo and the current GPS system is helpful in providing a better understanding of the needs of the European GNSS system. According to the Directorate-General for Energy and Transport within the European Commission (EC), it is crucial for Europe to have an option independent of the current U.S.-GPS monopoly, which is less advanced, less efficient, and less reliable. As stated by the Commission, the specific drawbacks of GPS are identified as:

- **Mediocre and varying position accuracy** Depending on the time and place, GPS accuracy is sometimes given within "several dozen metres." From a European perspective, this inaccuracy is blatantly insufficient, particularly within the transportation sector. With its better precision, Galileo is set to fill this gap.
- **Questionable geographic reliability** In northern regions that are frequently used as aviation routes, GPS provides limited coverage. This also affects the coverage accuracy in northern Europe, which

includes several EU member states. In addition, Galileo would boost overall urban coverage from the current rate of 50 percent (provided by GPS alone) to 95 percent.

- **Questionable signal reliability** With GNSS services playing a significant role in society, there is concern about the possibility of service shutdown. If the GPS system became dysfunctional or was turned off (accidentally or not), it has been conservatively estimated that the cost to European economies would be between €130 and €500 million per day.

1.2.4.2 Receiver Improvements A GPS/Galileo receiver offers a range of new services not currently available. The interoperability between GPS and Galileo will present new possibilities beyond the realm of imagination. Including Galileo technology in the receiver would not only improve the accuracy down to the centimetre and maintain current services, it would also improve the following:

- **Data integrity** This opens a broad range of applications for different products, especially for those where data integrity is critical, such as user authentication. Other examples include, but are not limited to, security applications, the surveillance and transporting of dangerous or sensitive goods, and railway transport security.
- **Emergency management** Galileo technology can help avoid sudden accidents or speed up emergency assistance vehicles when required.
- **Rescue services** Galileo technology could locate specific boats, planes, and vehicles after an accident, especially in the wake of natural disasters.
- **Data confidentiality** Applications depending on data confidentiality will be possible because of information encryption's compatibility with Galileo.
- **Advanced assistance** Galileo is capable of using an auto-pilot feature for remote control of motor vehicles.

Galileo is a civil service, which ensures constant signal availability, while GPS could be stopped at any time for any military emergency, which would result in economic losses. Galileo improves information accuracy and continuity as well as service availability. It is especially useful for locating users in hostile environments such as geographically rugged or highly developed urban locations.

Finally, it is worthwhile to point out that to carry out the aforementioned developments, it will be technologically necessary to introduce new, small, low-cost, highly autonomous dual receivers (GPS/Galileo).

1.3 State-of-the-Art GNSS RF Front-End Receivers

A review of current state-of-the-art GNSS radio frequency (RF) front-end receivers is required to establish the starting point in the creation of any electronic device. Not only have scientific papers been published on GNSS front-end receivers but a number of these devices are also on the market. Thus, both scientific papers and commercial receivers will be analysed.

1.3.1 Scientific Papers

An integrated GPS front-end was first mentioned in scientific literature in 1992[Benton92]. It was designed with gallium arsenide (GaAs) technology and was capable of a 54dB gain at 1600mW, with a low noise amplifier (LNA) of 2.7dB, as shown in Table 1-4.

As usual, GaAs technology played an important role in the early stages of these devices. As soon as bipolar and complementary metal-oxide semiconductor (CMOS) performance improved, designs adapted these technologies. Thus, from 1997 on, all published designs have been either bipolar, CMOS, or silicon germanium (SiGe). Although CMOS makes up the majority of designs, two bipolar references, [Kucera98] and [Cloutier99], have been found and only one of the designs uses SiGe technology[Sivonen02]. There is still a debate about which technology, CMOS or SiGe, is the most suitable for RF applications. Although SiGe performs better than CMOS when it comes to RF, the latter is the more affordable of the two. Furthermore, the lowest noise figure (NF) for the LNA is achieved with SiGe technology[Sivonen02].

A brief analysis of the front-ends can be found in Table 1-4. As reflected in the table, some of the front-ends make use of an external LNA as in [Murphy97] and [Piazza98]. Although the LNA has a high gain, it also presents high NF throughout the entire system. Other designs such as [Shahani97], [Svelto00], and [Sivonen02] do not integrate a phased-lock loop (PLL), voltage-controlled oscillator (VCO), or analogue to digital converter (ADC) and consequently consume less power. Due to integration complexity, most of them have both external intermediate frequency (IF) filters and RF filters[Sainz05]. Finally, the digitalization for most of the designs is carried out by a 1bit ADC.

[Chen05] and [Sahu05], which employed CMOS 0.18um and CMOS 90nm respectively, do not match the gain and NF performance found in [Shaeffer98] and [Kadoyama04], both of which also made use of CMOS technology and are highly integrated. The second one exhibits lower power consumption and includes the correlator and processor in the same chip, making it suitable for mobile applications. The main characteristics of the GPS front-ends collected here are summarized in Table 1-4.

TABLE 1-4 State-of-the-art GPS front-ends

Reference	LNA NF [dB]	chip NF [dB]	Gain [dB]	P1dB [dBm]	IIP3 [dBm]	Power consumption [mW]	Technology	Architecture	External components	ADC
[Benton92]	2.7	—	54	—	—	1600@8V	GaAs	Digit. IF	—	—
[Murphy97]	2	6.1	107	–29	—	81@3V	Bipolar	Hetero	Filters, LNA, PLL	1bit
[Shahani97]	3.8	—	13	—	—	12@1.5V	CMOS 0.5µm	Digit. IF	Filters, VCO, PLL, ADC	—
[Kucera98]	2.3	3.5	20	—	—	16.5@3V	Bipolar	—	—	—
[Piazza98]	1.5	8.1	94.5	–28	—	32@3V	BiCMOS 1µm	Hetero	2 filters, LNA	1bit
[Shaeffer98]	2.4	4.1	98	–58	—	112@3V	CMOS 0.5µm	Digit IF	Filters	1bit
[Cloutier99]	3	4	120	—	–26	49@3V	Bipolar	-----	Filters	2bit
[Meng98]	2.4	5.4	82	—	—	79	CMOS 0.5µm	Digit. IF	VCO, PLL	1bit
[Svelto00]	—	3.8	40	—	–25.5	8@2.8V	CMOS 0.35µm	—	Filters, VCO, PLL, ADC	—
[Sivonen02]	1.38	2.7	25.8	–27.6	–14.5	15.3@2.7V	SiGe	—	Filters, PLL, ADC	—
[Steyaert02]	1.5	—	15.5	—	–6	—	CMOS 0.25µm	—	—	—
[Kadoyama04]	—	4	110	—	—	27@1.8V	CMOS 0.18µm	—	Filters	1bit
[Chen05]	—	4.13	27.7	–29.9	–19	22.2@1.8V	CMOS 0.18µm	—	—	—
[Sahu05]	1.8	2	38	—	—	60@1.4V	CMOS 90nm	—	—	—
[Berenguer06]*	3.2	3.7	103	—	—	62@3V	SiGe 0.35µm	Low IF	Filters	1bit

*GPS/Galileo front-end.

The latest reported GPS front-end [Berenguer06] is the only device that could currently be applied to GPS and Galileo. It encompasses 0.35um SiGe technology, exhibits a high voltage gain of 103dB, a single-sideband modulation (SSB) noise level of 3.7dB (which makes it suitable for high-sensitivity applications), a power consumption of only 62mW from a 3V supply, and a minimal amount of external components (which makes it suitable for mobile applications).

1.3.2 Commercial Receivers

Many semiconductor companies offer a GPS receiver chipset. Out of all the reviewed commercial receivers, only [ublox ATR0630_35] includes the baseband processor together with the RF front-end; the rest are mostly composed of two integrated circuits (ICs): the front-end and the processor. A comparison of characteristics of front-ends from different manufacturers is summarised in Table 1-5.

Although most devices described in scientific papers are designed with CMOS, most commercial front-ends use bipolar technology. Not all

TABLE 1-5 State-of-the-art GPS commercial IC front-ends

Reference	VCC [V]	Power [mW]	Gain [dB]	NF [dB]	Bit nr.	Comments
[Atmel ATR0603]	3	38	76	8	1	External LNA, single conversion, AGC
[Freescale MRFIC1505]	3	84	105	2	—	Internal LNA, double conversion, AGC, no ADC
[MAXIM MAX2741]	3	90	80	4.7	2/3	Internal LNA, double conversion, AGC
[MAXIM MAX2769]	3	54	96	1.4	2/3	Two internal LNA, single conversion, ready for Galileo
[PHILIPS UAA1570HL]	3	165	148	4.5	1	Two internal LNA, double conversion, AGC
[SiGe SE4120L]	3	30	18	>1.6	—	Internal LNA, ready for Galileo, multibit serialized digital I/Q output
[SONY CXA1951AQ]	3	90	100	7	—	Internal LNA, double conversion, no ADC
[ST STB5610]	3.3	122	139	3	1	Internal and external LNA, single conversion
[ublox ATR0630_35]	3	87	90	6.8	1.5	Integrated solution including RF, IF filter, and baseband
[uNAV un8021C]	3	62	~106	20	2	Internal LNA, single conversion
[zarlink GP2015]	3	173	120	9	2	External LNA, triple conversion, AGC

systems are fully integrated, since the LNA is external in some cases. Moreover, mainly 1bit and 2bit ADCs are used for digitalisation.

The [ST STB5610] front-end presents the best gain-to-noise figure ratio with a gain of 139dB and an NF of 3dB, achieved at a rate of consumption as high as 122mW. [Freescale MRFIC1505] also has a high gain of 105dB with a low NF of 2dB. On the other hand, [uNAV un8021C] achieves a gain of 106dB while consuming 62mW. However, it presents a high NF of 20dB. [SiGe SE4120L] and [MAXIM MAX2769] are dual front-ends currently ready for GPS and Galileo applications.

1.3.3 Components

A thorough analysis of available key components of a front-end such as the LNA, mixer, and PLL is required prior to the definition of the front-end blocks to be designed. The reviewed scientific papers and datasheets failed to provide all required information.

First, characteristics of some LNAs of the previously mentioned front-ends are shown in Table 1-6. Most of the designs are single-ended designs and work with a power supply between 1.5V and 3.3V. The most important characteristics to consider are noise, gain, and power consumption. The highest gain is achieved by [Shaeffer97], which exhibits 20dB with a 3.5dB noise level. On the other hand, the lowest noise level is achieved in the first LNA of the two included in [MAXIM MAX2769], which exhibits 0.83dB for a 19dB gain.

Table 1-7 shows the characteristics of the mixers of some of the previously mentioned GPS front-ends. Conversion gain, noise, and power

TABLE 1-6 State-of-the-art LNAs for GPS

Reference	Vdd [V]	Current [mA]	Gain [dB]	NF [dB]	P-1dB [dBm]	IIP3 [dBm]
[Shaeffer97]	1.5	20	22	3.5	–24.5	–9.3
[Shahani97]	1.5	8	17	3.8	–21	–6
[Shaeffer98]	2.5	5	16	2.4	–23	–8
[Piazza-Orsati98]	2.5	18	14	2	–16.8	–1.5
[Sanav02]	2.5	4.5	19.5	1.3	—	—
[Maxim01]	3	5.8	15	1.5	–18	–3
[Alvarado07]	3	8	18	3.3	–24	—
[MAXIM MAX2769]	3	—	19	0.83	—	–1.1
[MAXIM MAX2769]	3	—	13	1.14	—	1
[PHILIPS UAA1570HL]	3	—	15.5	3.7	–22	–13
[ST STB5610]	3.3	—	19	3	—	–20
[Freescale MRFIC1505]	3	—	15	2	–14	—
[ublox ATR0610]	3	3.3	16	1.6	–9	–1

TABLE 1-7 State-of-the-art GPS mixers

Reference	Vdd [V]	Current [mA]	Gain [dB]	NF [dB]	P-1dB [dBm]	IIP3 [dBm]
[Kilicaslan97]	—	—	3.35	9	–12	2.17
[Sullivan97]	3	13	6.5	8.5	–12	–3
[Wang88]	1	—	6	9.6	–5	10
[PHILIPS UAA1570HL]	3	—	17.7	12	–25.4	–16.3
[zarlink GP2015]	3	—	18	9	–16	—
[Atmel ATR0603]	3	—	~20	6.9	—	—
[ST STB5610]	3	—	30	5.5	—	–19
[SONY CXA1951AQ]	3	—	16	7	—	—
[Freescale MRFIC1505]	3	—	14	13	–27	—

consumption are the key parameters for this component. The highest gain of 30dB and the lowest noise level of 5.5dB are obtained by [ST STB5610], made possible by a preamplifying stage prior to the mixer itself.

Finally, Table 1-8 includes not only PLLs of GPS front-ends, but also PLLs of other applications working at similar frequencies. The main parameters to take into account are the phase noise and the power consumption of the device.

1.3.4 Summary

Key parameters useful in comparing the quality of front-ends are gain, noise level, power consumption, integration ratio, and size. Thus, sensitivity, required space, and battery life can be determined. A comparison of available front-ends is worthwhile to set realistic competitive requirements for the desired front-end.

Most commercial front-ends have a high gain exceeding 100dB. The high gain is achieved at a cost of either a high noise level or high power consumption. The same can be seen with designs published in scientific

TABLE 1-8 State-of-the-art PLLs for GPS

Reference	Vdd [V]	PN [dBc/Hz]	Current [mA]
[Nhat92]	5	–88 @ 100kHz	14
[Craninckx95]	3	–115 @ 200kHz	8
[Craninckx98]	3	–123 @ 600kHz	3.7
[Hajimiri99]	3	–125 @ 600kHz	16
[Rogers00]	3.3	–96 @ 100kHz	6
[PHILIPS UAA1570HL]	3	–72 @ 10kHz	—
[ST STB5610]	3	–60 @ 10kHz	—
[Atmel ATR0603]	3	–100 @ 1kHz	—
[zarlink GP2015]	3	–88 @ 100kHz	—

papers; high gain is obtained at a cost of power or noise. However, the gain is lower than that found in commercial receivers.

High power consumption means shorter battery life and therefore less mobility. However, many applications are not power critical, as in the automotive industry, where the battery of the car could be used. A high noise level could mean lower receiver sensitivity, which is not a drawback in open spaces such as hiking paths free of trees or on the sea, where the battery of a mobile device plays a more important role. However, many applications require long battery life and high sensitivity, which essentially calls for a front-end with a high gain, low noise, and low power consumption.

1.4 Design Methodology

For any research project to succeed, clear objectives have to be defined. The more specific the objectives, the more likely they can be achieved. Specific objectives will be used to develop a GPS/Galileo front-end, the benefits of which will be described in this chapter. To ease reader comprehension, the contents and structure of this book are briefly explained.

1.4.1 Objectives

The main objective of this book is to describe a methodology in order to design, fabricate, and test a highly integrated, low-noise, low-power, and low-cost RF front-end prototype for both satellite-based global navigation systems, GPS and Galileo. As shown earlier in this chapter, this receiver will be a key component for accessing a variety of new services offered by these systems.

This main objective must be divided into intermediate goals that will lead to the design of the front-end. These have to be accomplished step by step; that is, once the first goal has been fulfilled, the second one will be ready to be tackled. The objectives to be carried out are as follows:

- A study of GPS and Galileo standards in order to set the requirements for the receiver.
- Specification of the receiver as a whole and the integrated circuit to be designed, particularly the features of the different blocks. It covers the technology, front-end, and receiver block architectures and selection of the necessary external components, and so on.
- Design of the receiver spanning from simulation to postlayout results that fulfil the previously defined specifications. It covers not only the receiver blocks, but also the internal logic and the electrostatic discharge (ESD) of the different input/output (I/O) PADs.

- On-wafer characterisation of the different circuits in the IC, including the passive components and the active circuits.
- Design and fabrication of the printed circuit board (PCB) for the final application.
- Measurement of the whole IC in order to validate the prototype.

Throughout this book, a dual GPS/Galileo RF front-end will be described as an example. This design hails from CEIT`s COMMIC group of the Electronics and Communications Department (www.ceit.es/electrocom/RF/), which has previous experience in researching GPS front-end receivers.

1.4.2 Benefits of the Receiver

The most promising objective of the proposed dual RF front-end is its compatibility with both GPS and Galileo. Thus, receiver accuracy will be improved, offering the user a range of new services not yet available. GPS/Galileo will change the way many people do their work. It will fundamentally alter business as we know it and provide opportunities for new applications we have not yet imagined.

Additional objectives are proposed to improve features and reduce costs compared to those of actual receivers existing on the market. Among the improvements, a high integration of the proposed architecture is intended; that is, it integrates components that previously were left out, minimising the number of external components needed. Component integration and external component minimisation offers the user a number of advantages: cost, size and weight reduction for the receiver, and at the same time lower power consumption, improvement of features, and reliability enhancement due to the drastic reduction of the number of interconnections and soldering. For users, this means longer battery life and higher receiver quality.

1.4.3 Book Structure

This book is arranged according to the logical order in which an IC should be designed. It consists of six chapters briefly described as follows.

This chapter serves as an introduction to and briefly takes a look at the history of Global Navigation Satellite Systems. It goes on to present the driving force of this book by showing the strength and versatility of a dual GPS/Galileo receiver. Moreover, a state-of-the-art GPS RF front-end is also included and both commercial and academic receivers are analysed. Finally, the methodology to be followed for the design is described, the benefits of the receiver are expounded, and the structure of this book is shown.

The second chapter deals with the specifications of the receiver. How its specifications have been obtained is described, beginning with a technical explanation and study of GPS and Galileo. With the introductory to specifications, the third chapter shows the design of all the IC blocks, including the receiver chain, PLL, control logic, and PADs, as well as the front-end and its component architectures. In addition, the floor planning of the entire IC is shown. Then, the fourth chapter deals with the characterisation of the fabricated devices designed in the previous chapter. It illustrates the procedures taken to measure them as well as the entire front-end. The fifth chapter names some fields that will benefit from such a receiver, and shows an application module for cars that includes the RF front-end design example described in detail in this book. Conclusions to this book are summarised in the sixth chapter. Finally, the bibliography referenced throughout the book is also listed.

Chapter

2

Receiver Specifications

This chapter deals with the specifications of the dual GPS/Galileo RF front-end. As the starting point for the design of the RF front-end, a study of the technical issues related to the signals of the GPS and Galileo standards is shown. This is employed to obtain the specifications of an interoperable dual GPS/Galileo RF front-end, which is explained in the second part of this chapter.

2.1 Global Navigation Satellite Systems

In this chapter, the GPS and Galileo standards are explained in more detail. Specifications of the RF front-end must be determined in response to the signals transmitted by the satellites.

2.1.1 Global Positioning System (GPS)

The development of the Navstar GPS took nearly 20 years and cost more than $10 billion. It is the first and currently the only fully operational Global Navigation Satellite System (GNSS). The GPS project began in 1973 and attained full operational capability (FOC) in 1995, although it was already in use at the beginning of the 1980s. Developed by the U.S. Department of Defense (DoD), GPS is intended to serve as primary means of radio navigation well into the twenty-first century. GPS replaced less-accurate systems such as LORAN-C, OMEGA, VOR, DME, TACAN, and Transmit.

GPS has become much more than a military navigation platform since it has been opened to civilian use. Many new civil applications have appeared over the last few years in response to the decreasing cost, size, and power consumption of GPS receivers. Moreover, receiver capabilities continue to improve and small multichannel receivers with

sophisticated tracking, filtering, and diagnostic features are making even advanced applications possible.

The civil uses of GPS include, but are not limited to, marine and aviation navigation, precision timekeeping, surveying fleet management (rental cars, taxis, delivery vehicles), aircraft approach assistance, geographic information systems (GIS), wildlife management, natural resource location, disaster management, meteorological studies, and recreation (hiking and boating)[HP AN1272].

2.1.1.1 Architecture Any GNSS consists of three different parts, namely the space segment, ground segment, and receiver. The space segment is composed of the satellites in space, whereas the ground segment controls the operation of the system from the Earth. Varying degrees of accuracy and services can be obtained depending on the receiver in use.

The GPS space segment is comprised of 24 Navstar satellites (and one or more in-orbit spares) distributed throughout six orbital planes. It takes 12 hours for the satellite to orbit the Earth, during which time it will have travelled 10900 nautical miles (approximately 20200km) orbits, meaning that each satellite passes over the same location on the Earth roughly once a day. Normally, five satellites are within range of users worldwide at any given moment. During the last 28 years, four different generations of GPS satellites have been developed: Block I, Block IIA, Block IIR (replenishment), and Block IIF (follow-on). The average lifespan of the first three generations of satellites is from 7 to 10 years, while the last generation is expected to last 15 years.

First launched in 1997, Block IIR satellites make up the majority of the current constellation of satellites. Block IIR satellites are equipped with an auto-navigation capacity (AUTONAV) that allows each spacecraft to maintain full positioning accuracy for at least 180 days without Control Segment support. The latest satellites in this series (Block IIR-M) carry a new military code or M-code. The M-code will be more jam-resistant than the current military GPS code (also known as P-code). In addition, these satellites will offer a second civil signal on the L2 band. Beyond the Block IIR-M, there are also plans to upgrade the system through the introduction of the GPS IIF programme (its first launch is planned for 2008). The Block IIF programme will transmit a third civil signal on the L5 band. A fifth generation of GPS satellites, Block III, is expected to dramatically enhance the performance of the system. It will add a third signal on the L1 and L2 bands (for which the first launch is planned for 2012). These satellites will provide a more resistant, accurate, and reliable signal through increased transmission power.

The ground segment consists of different stations scattered throughout the world. A master control station in Colorado Springs controls the space segment. In addition to operating the master control station,

the United States operates five unmanned monitor stations and four ground antennas to pick up GPS satellite signals. The data collected by the monitor stations are used to calculate positioning corrections for the satellites. This process ensures the synchronisation of the satellites and the accuracy of the signals sent to the Earth.

2.1.1.2 GPS Signals and Services There are two types of GPS terminals, categorised according to the code they can acquire. The services available depend on the code received. Therefore, depending on the receiver, the offered services are as follows:

- **Standard Positioning Service (SPS)** This service is available freely to the general public for civilian applications. Position is set by using the coarse acquisition (C/A) signal.
- **Precise Positioning Service (PPS)** PPS receivers are used exclusively by authorised government agencies. Military receivers do not have to go through the C/A signal to track the P(Y) signal. Then, once military personnel is equipped with PPS receivers, C/A signal can be switched off on the battlefield without fear of repercussions for friendly military forces[Kaplan96].

2.1.1.3 Currently Transmitted Signals A GPS satellite currently sends signals L1 and L2 with a central frequency of 1575.42MHz for L1 and 1227.6MHz for L2, as shown in Figs. 2-1 and 2-2. There is a third signal, defined as L3, sent by satellites with a central frequency of 1382.05MHz. This signal will not be covered in this book due to the fact that it is employed by the Nuclear Detonation Detection System (NUDET) and has no navigation finality.

Figure 2-1 shows how L1 and L2 are built. The L1 signal is a QPSK signal modulated in phase by the C/A-code and the information of the navigation message, and in quadrature by the precision code (P-code) and the navigation message. The L2 signal is a BPSK or QPSK signal modulated by a single signal, the C/A-code, the P-code, or the P-code and the information of the navigation message, depending on the selector position.

Figure 2-2 shows the baseband spectrum of the signals for a normalised transmitted power of 1W while Eq. 2-1 and Eq. 2-2 express the signals analytically.

$$S_{L1}^{(k)}(t) = \sqrt{2P_C} \cdot D^{(k)}(t) \cdot x^{(k)}(t) \cdot \cos(2\pi f_{L1} t + \theta_{L1}) + \sqrt{2P_{Y1}} \cdot D^{(k)}(t) \cdot y^{(k)}(t) \cdot \cos(2\pi f_{L1} t + \theta_{L1}) \quad (2\text{-}1)$$

$$S_{L2}^{(k)}(t) = \sqrt{2P_{Y2}} \cdot D^{(k)}(t) \cdot y^{(k)}(t) \cdot \sin(2\pi f_{12} t + \theta_{L2}) \quad (2\text{-}2)$$

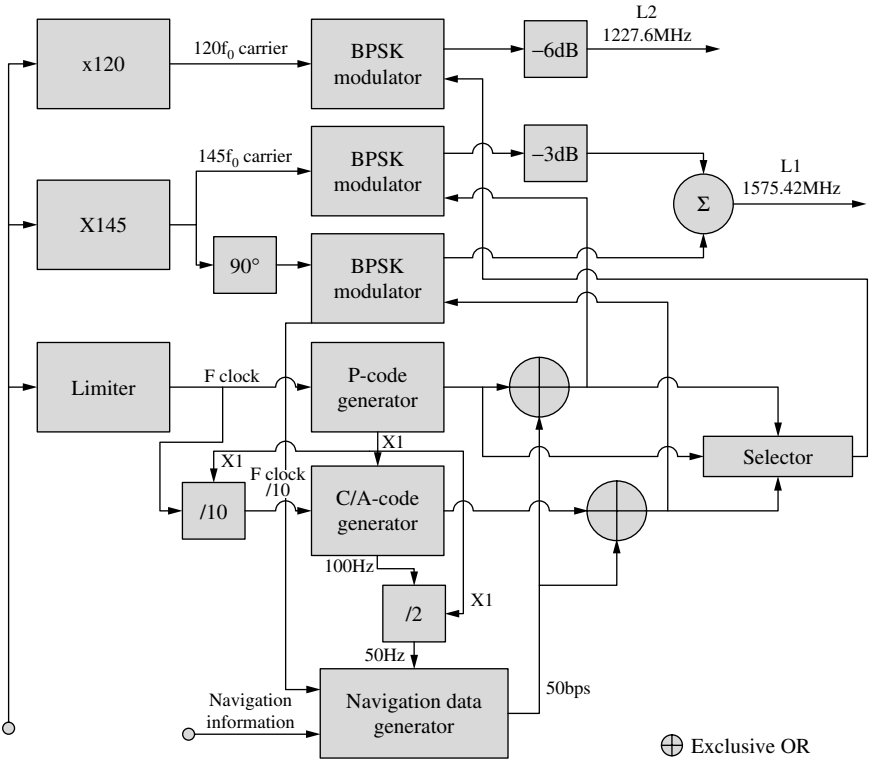

Figure 2-1 Signals sent by a GPS satellite

In Eq. 2-1 and Eq. 2-2, the square root is the signal amplitude (sqrt($2P_c$)), $D^{(k)}(t)$ is the navigation message, $x^{(k)}(t)$ and $y^{(k)}(t)$ are the acquisition codes (spread spectrum codes), and f_{L1} is the carrier frequency.

The coarse acquisition code C/A is also a pseudorandom noise (PRN) code with a clock frequency of 1.023MHz. It is the basis for the code-division multiple access (CDMA), used to send the signal from the satellites to the receivers. Every satellite has a unique C/A-code. These signals are detected and then separated through these codes, which have high-quality cross-correlation properties. This acquisition code constitutes the basis for the service used by the civilian SPS.

The P-code is a 10.23MHz frequency PRN code It is unique for each satellite and used for codification purposes. As PPS bases its service on this code, it is exclusively for military use.

This book focuses on the civilian use of the receiver. Thus, the frequency band considered is the one due to the C/A-code, plus the navigation message, which is 2.046MHz centred on the 1575.42MHz frequency. The signal located on the L2 band will not be considered for the dual

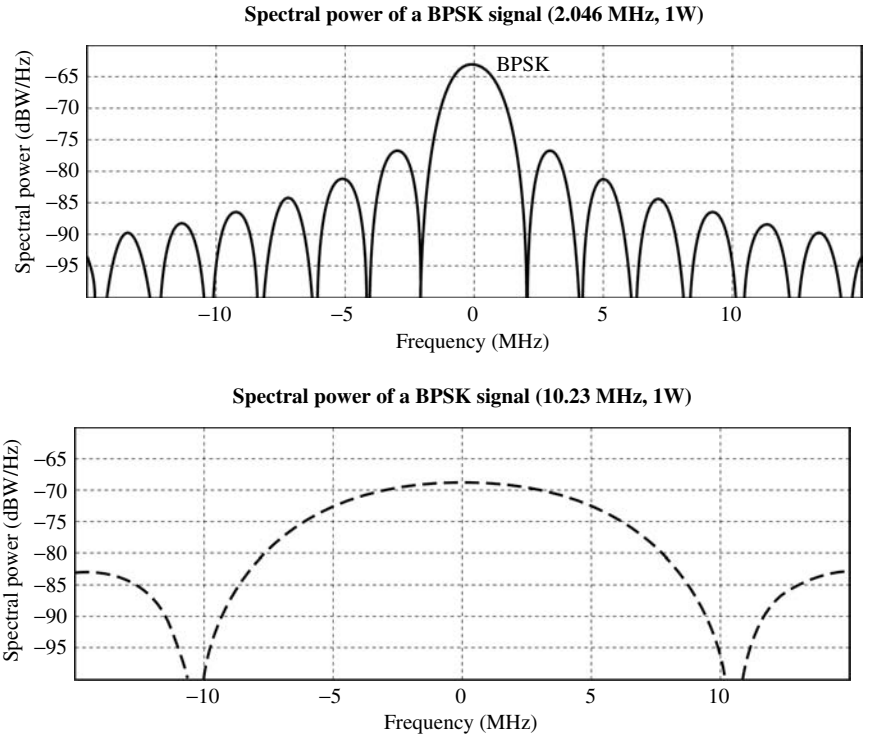

Figure 2-2 (a) L1 signal spectrum; (b) L2 signal spectrum

GPS/Galileo RF front-end dealt with in this book. Commercial receivers only employ the L1 band. Before 1 May 2000, employing the C/A-code on L1 and with the Selective Availability switched on, the 3D accuracy was around 25-100m, 95 percent of the time. Nowadays, employing the C/A-code on L1, and with the SA set to 0 the 3D accuracy, it is around 6-11m 95 percent of the time. New civil signals will offer an improved accuracy, integrity and continuity of service.

2.1.1.4 Planned Signals for the Future The U.S. DoD is planning to renew the GPS satellite constellation. Twenty-nine new satellites are being launched between 2003 and 2012. These satellites will send not only current signals but also additional ones that will allow more accurate and reliable positioning.

Four new signals are expected to be used: two for military purposes on the L1 and L2 bands, and two for civil use on the L2 band and the new L5 band. Since this book is not focused on military applications, only those signals used by civilians are discussed in this section.

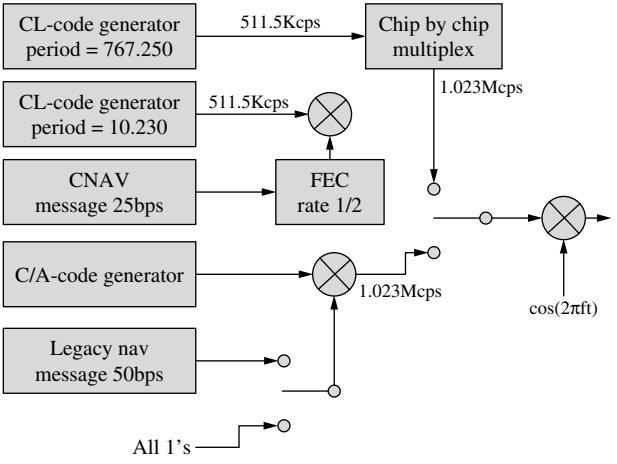

Figure 2-3 L2 sent by GPS satellites

The L2 signal sent by new satellites can be expressed analytically as follows:

$$S_{L2}^{(k)}(t)=\sqrt{2P_{Y2}}\cdot D^{(k)}(t)\cdot y^{(k)}(t)\cdot\cos(2\pi f_{L2}t+\theta_{L2})$$
$$+\sqrt{2P_C}\cdot F[D^{(k)}(t)]\cdot RC(t)\cdot\cos(2\pi f_{L2}t+\theta_{L2})+M \qquad (2\text{-}3)$$

where the first term represents the signal being currently sent as shown in Eq. 2-3. The second term represents the signal for civilian use. The generation of the signal, a 1227.6MHz (f_{L2}) frequency signal modulated by two codes, is shown in Figure 2-3. Navigation messages are coded by Forward Error Correction (FEC) techniques. The last term represents the new signal for military purposes, the details of which are unknown.

The new signal uses C/A-code or another different one from what it is used now, the replacement code (RC), as acquisition code. The C/A is a PRN-code with a clock frequency of 1.023MHz. Compared to C/A, the new RC-code is significantly longer.

By means of this signal and the one on the L1 band, a civilian receiver will be able to correct delays caused by the ionosphere and troposphere, offering more accurate positioning than they do now.

Figure 2-4 shows the spectrum for the new signal of the L2 band. Signal bandwidth is 2.046MHz, the same as the civilian signal of the L1 band.

The L5 signal will be transmitted by the new satellites (from Block IIF) and can be expressed analytically as follows:

$$S_{L5}^{(k)}(t)=\sqrt{2P_G}F\left[D_{L2}^{(k)}(t)\right]NH_{10}(t)g_1^{(k)}(t)\cos(2\pi f_{L5}t+\theta_{L5})$$
$$+\sqrt{2P_G}NH_{20}(t)g_2^{(k)}(t)sen(2\pi f_{L5}t+\theta_{L5}) \qquad (2\text{-}4)$$

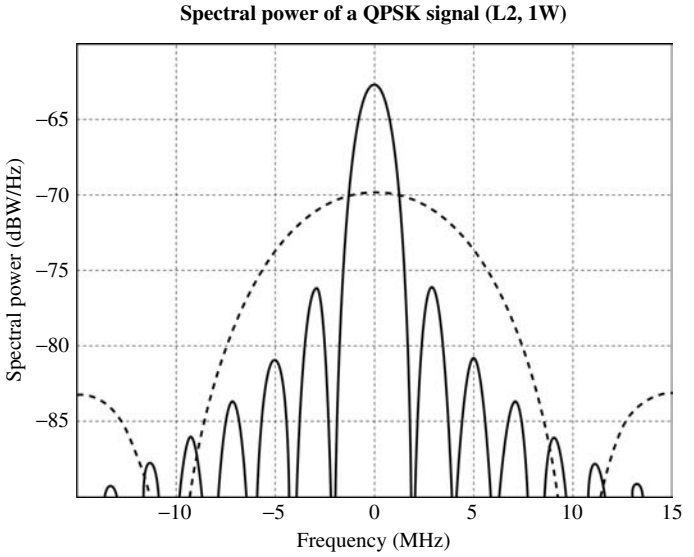

Figure 2-4 Spectral power of the L2 band's new signal

It is a QPSK signal phase modulated by $g_2(t)$ and $NH_{20}(t)$ codes and in quadrature by $F[D_{L2}{}^{(k)}(t)]$, $NH_{10}(t)$, and $g_1{}^{(k)}(t)$ codes. The codes $g_1(t)$ and $g_2(t)$ are PRN codes with a clock frequency of 10.23MHz. Thus, the bandwidth of the RF-modulated signal is 20.46MHz. $NH_{10}(t)$ and $NH_{20}(t)$ are Neumann-Hoff codes with a clock frequency of 10.23MHz. They increase the size of the $g_1{}^{(k)}(t)$ from 10230chips to 1023000chips and $g_2{}^{(k)}(t)$ from 10230 chips to 204600chips. The carrier frequency (f_{L5}) is 1176.45MHz.

Figure 2-5 shows how to obtain the new L5 signal and Figure 2-6 illustrates the spectrum of the signal.

As in the case of the L2 band signal, the signal on the new L5 band can be used together with the L1 band signal to eliminate the effect of

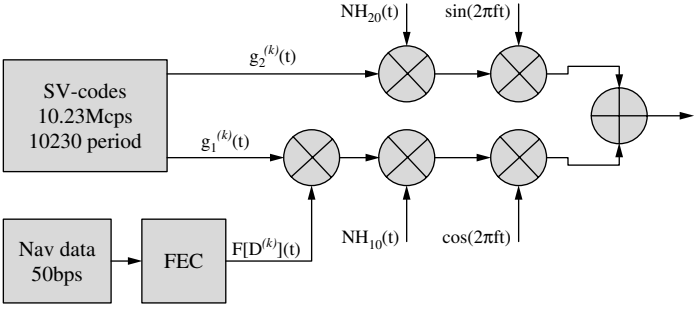

Figure 2-5 Signal L5 sent by GPS satellites

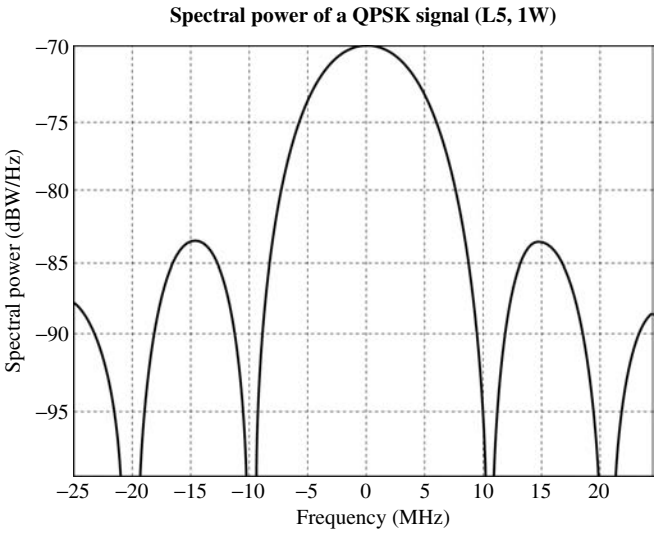

Figure 2-6 Spectral power of the new signal on the L5 band

the delays caused by the ionosphere and troposphere, thus obtaining more accurate positioning.

Moreover, Block III satellites will add a new civilian signal, called L1C, which will be transmitted on the L1 carrier frequency in addition to the C/A-code signal. The development of L1C represents a new stage for GNSS; the signal is not only designed for GPS transmission, it will also be interoperable with Galileo's Open Service signal centred on the same frequency[Betz06].

2.1.1.5 Description of GPS Signals Table 2-1 briefly shows the current signals of GPS satellites and the signals of the new generation, planned to be in use starting in 2012.

TABLE 2-1 Signals sent by the new GPS satellite constellation [ARINC00]

Frequency band	L1	L2	L5
Channels	A B C	A B C	I Q
Frequency	1575.42MHz	1227.6MHz	1176.45MHz
Modulation type	A,B → QPSK C → BOC(1,1)	A,B → BPSK or QPSK C → BOC(10,5)	QPSK
Bit rates	A → 1.023MBs B → 10.23MBs C → 1.023MBs	A → 1.023MBs B → 10.23MBs C → 5.115MBs	I,Q → 10.23MBs
Minimum received power @ elevation 10°	A → −131dBm B → −128dBm C → −127dBm	A → −134dBm B → −130dBm C → tbd	I,Q → −128dBm

In the future, civilian users will be offered three kinds of receivers depending on their location accuracy[ARINC00]:

- Current receivers will still work with the same accuracy as now tens of metres, and should be sufficient for certain applications.
- Dual receivers that receive and process two signals, L1 and L2 or L1 and L5, will be more accurate, metre level. This is achieved by correcting delays caused by the ionosphere and troposphere, offering more accurate positioning.
- High-accuracy receivers will make use of signals L1, L2 and, L5. These kinds of receivers will offer centimetre-level accuracy and will be required to be differential.

2.1.2 Galileo

In 1998, the European Space Agency (ESA) and the European Commission jointly decided to study the feasibility of a truly independent European GNSS. Named Galileo, the program was first approved in 1999. Besides being independent, Galileo is expected to offer greater accuracy, integrity, availability, and continuity of services compared to present systems. In spite of the dual-use nature of any GNSS system, Galileo is intended for civilian application only. It has been deemed a "civil programme under civil control."

Being civilian-friendly means that, so far, none of Galileo's funding has come directly from defence budgets. With deployment costs estimated between €3.2–3.6 billion, funding is expected to come from public-private partnerships (PPP) and fee-for service charges to be collected by the Galileo Operating Company (GOC). Total costs, including 12 years of operational costs, are likely to reach €6 billion. With respect to partnerships, the European Investment Bank and a number of private enterprises are collectively planning to pledge a minimum of €5 million to the project. They may team up with Joint Undertaking (JU), which is presently responsible for the development and validation phase. To avoid conflicts of interest, private enterprises may not become members until the tendering process has finished.

2.1.2.1 Architecture Like any GNSS, Galileo consists of the space segment, the ground segment, and the user receiver. The space segment will be comprised of 30 satellites (27 active and 3 spare) in the Medium Earth Orbit (MEO) at an altitude of 23600km. The satellites will travel along three circular orbits at an inclination of 56°, ensuring global coverage. With a satellite orbit time of 14 hours, the configuration of the constellation will guarantee at least six in-sight satellites at any given time for any location, including the poles.

The Galileo satellites will have an expected lifespan of 10 years. Individual satellites will be replaced on a regular basis to account for eventual malfunctioning, residual life, and accommodation of future payload technology.

The space segment will be managed by two control centres located in Europe, supported by 20 Galileo Sensor Stations (GSS). Data exchanges between the control centres and the satellites will be carried out through specific uplink stations. A total of 15 uplink stations will be installed around the world to facilitate this type of data transfer. As the principal component of the ground segment, the control centres will be responsible for the management of the satellites, the integrity of the signals, and the synchronisation of the atomic clocks onboard the satellites.

2.1.2.2 Galileo Signals and Services Galileo satellites will transmit ten different signals located on the following bands: E5a and E5b (1164–1215MHz), E6 (1260–1300MHz), and E1-L1-E2 (1559–1592MHz). Six signals will be devoted to civilian (Open Service) and Safety of Life (SoL) services, two for commercial users, and the remaining two (Public Regulated Services, or PRS) for official/regulated personnel. Apart from these timing and navigation transmissions, Galileo will provide information concerning the accuracy and status of its signals. Known as "integrity messages," these signals are specifically geared for SoL applications, although they are likely to be offered to service industries requiring legal guarantees (during the transportation of valuable goods, for example). The services offered by Galileo are as follows:

- The Open Service (OS) will be available to civilian users free of charge and will accurately provide positioning, speed, and UTC time. According to the plans of the European Commission, the quality of the OS will be better than that of the present and future GPS civil services. It will be offered by the E5a, E5b, and E1-L1-E2 bands.
- The Commercial Service (CS) will operate under a fee-for-service plan. As such, access to the CS will require a payment to the GOC through the service provider in return for the encryption keys required to receive the signals. Compared to the OS, CS signals will be of a higher quality and will guarantee a certain level of reliability and accuracy. Service will be provided by signals located on E5b, E6, and E1-L1-E2 bands.
- The SoL service will offer the same accuracy as the OS but with a high level of integrity. A greater level of integrity is required for an effective and accurate service for companies working in the field of air and maritime navigation. At some stage, SoL may be encrypted and therefore require a fee for access. The Search and Rescue (SAR) service will be a certified service developed in accordance with

international regulations. It will provide real-time transmissions of emergency requests to facilitate the location of distress messages. SoL will be provided by the signals on the E5a, E5b, and E1-L1-E2 bands and will be a restricted service.

- The Public Regulated Services (PRS) signal will be for governmental use only and is designed to guarantee continuous signal access in the event of threats or crisis. It will require noncommercial receivers that can store the needed decryption keys and will be provided by signals on the E6 and L1 bands. An access-regulated service such as the SoL will also be required.

The goal of this book is to explain the design process of a receiver that will offer basic services to the user. Thus, signals on the E5a, E5b, and E1-L1-E2 bands that make up the Open Service will be described in detail.

2.1.2.3 Signals on the E5 Band Four different signals are sent on the E5 band with a central frequency of 1191.795MHz; E5a and E5b have two components in quadrature each one. The signal modulation is the alternative BOC, AltBOC(15,10). The signal processing techniques required to process AltBOC modulation are much more challenging than those used for traditional BPSK or even for usual BOC modulation. This stems from the extremely large bandwidth and from the complex interaction of four components of the spreading code. It can be assumed that the four signal components on the E5 band are modulated as a single wideband signal generated following AltBOC(15,10) 8-PSK modulation. This wideband signal is centred on the E5 frequency of 1191.795MHz and has a bandwidth of at least 70MHz. AltBOC modulation offers the advantage that the E5a (I&Q) and E5b (I&Q) bands can be processed independently, like traditional BPSK(10) signals, or together, leading to tremendous performance in terms of tracking noise and multipath functions. Characteristics of all four signals are summarized in Table 2-2.

2.1.2.4 Signals on the E1-L1-E2 Band The E1-L1-E2 band is composed of three channels sent by the same carrier (f_{L1} = 1575.42MHz) and modulated through the "modified hexaphase modulation." In baseband, channels B and C will show a BOC(1,1) modulation, while coded information will be sent through flexible modulation BOC(15,2.5) on channel A.

TABLE 2-2 Characteristics of the components of the E5 signal band

Signal component	Modulation	Data	Centre frequency
E5aI	BPSK(10)	Yes	1176.45MHz
E5aQ	BPSK(10)	No	1176.45MHz
E5bI	BPSK(10)	Yes	1207.14MHz
E5bQ	BPSK(10)	No	1207.14MHz

TABLE 2-3 Signals sent by Galileo satellites

Frequency band	E1-L1-E2	E5
Channels	A B C	I Q
Frequency	1575.42MHz	1164–1214MHz
Modulation type	B,C → BOC(1,1) A → flexible BOC(15,2.5)	AltBOC(15,10)
Bit rates	A → max 1.023MBs B,C → 2.046MBs	I,Q → 10.23MBs
Minimum received power @ elevation 10º	A → –125dBm B,C → –128dBm	I,Q → –128dBm

2.1.2.5 Description of Galileo Signals Table 2-3 summarises the signals of the Galileo satellites that provide the OS. The service will be operative starting in 2012.

2.1.3 GPS and Galileo Interoperability

After analysing the signals of the GPS and Galileo navigation systems, it can be seen that there are two frequency bands where both systems simultaneously send the navigation message: GPS L1 with Galileo E1-L1-E2 and GPS L5 with Galileo E5 (see Figure 2-7). A GPS/Galileo multistandard terminal should receive signals from one or both frequency bands and be able to provide the position with one or both systems at the same time.

This book aims to show the design process of a RF front-end that receives the signals of the first frequency band, namely GPS L1 and Galileo E1-L1-E2, so the receiver can relay position data with one or both systems at the same time. As the E1-L1-E2 signal bandwidth (24MHz) is higher than the L1 signal (2.046MHz), the former will establish the bandwidth of the input signal that has to be processed.

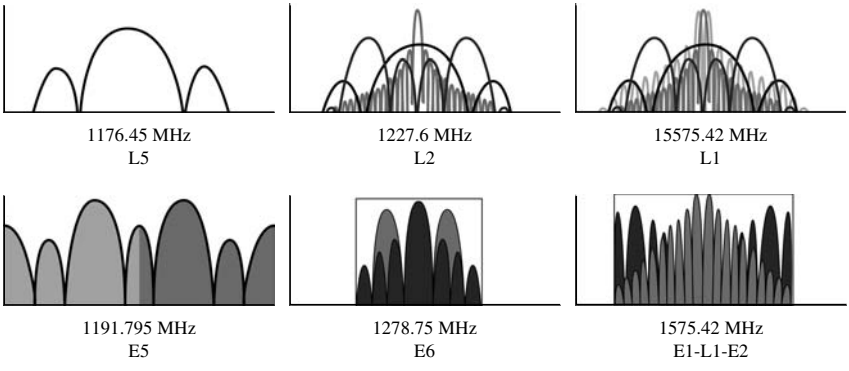

Figure 2-7 Signals bands sent by Galileo [Chatre05] and GPS [Stansell06]

Once the signals to be received by the front-end are identified, requirements for the receiver have to be defined. Specifications regarding noise, linearity, and bandwidth must be studied to obtain a reliable and accurate positioning through GPS and/or Galileo.

2.2 System Analysis

This section deals with the establishment of the specifications for a dual RF GPS/Galileo RF front-end, which is required for proper design and fabrication. The receiver's noise figure, third-order intermodulation product (IP3), and bandwidth requirements are taken from the GPS and Galileo standards analysed in the previous section. These parameters typically determine sensitivity, the lowest signal power that can be received; linearity, which is related to highest signal power that can be received and the frequency bandwidth of the receiver. All these parameters are related to the positioning accuracy and integration time through the BER as it is shown in the Figure 2-8.

The manner in which these are obtained is explained in detail in this section, along with the receiver architecture and the receiver blocks: receiver chain and phase-locked loop (PLL) specifications.

2.2.1 System Specifications

As with any other RF front-end, the parameters that characterise the receiver are the noise figure, linearity, and frequency bandwidth, which will be explained in the following subsections.

2.2.1.1 Noise Figure GNSS signals are transmitted by medium power satellites, with approximately 40dBm. When they reach the Earth, they are normally received by low-gain, low-power quasi-omnidirectional antennas with a minimum power of approximately –131dBm. Thus, multiple-access noise can be considered second-order noise rather than thermal or white noise. Moreover, [Parkinson96] explains that the transmission channel adds only Gaussian-distributed white noise.

First of all, the BPSK-modulated GPS L1 signal is considered. The error probability for the demodulation of a BPSK signal sent through a channel that considers Gaussian distributed noise can be calculated by Eq. 2-5.

$$P_E = erfc\sqrt{\frac{2E_b}{N_0}} = erfc\sqrt{\frac{2P_sT_d}{N_0}} = erfc\sqrt{\frac{2C}{N_0 f_d}} \tag{2-5}$$

where E_b is the energy per bit, P_s is the power of the received signal, C is the power of the received signal in 1Hz, and f_d is 50bps of the navigation message. This provides a valuable parameter to measure the

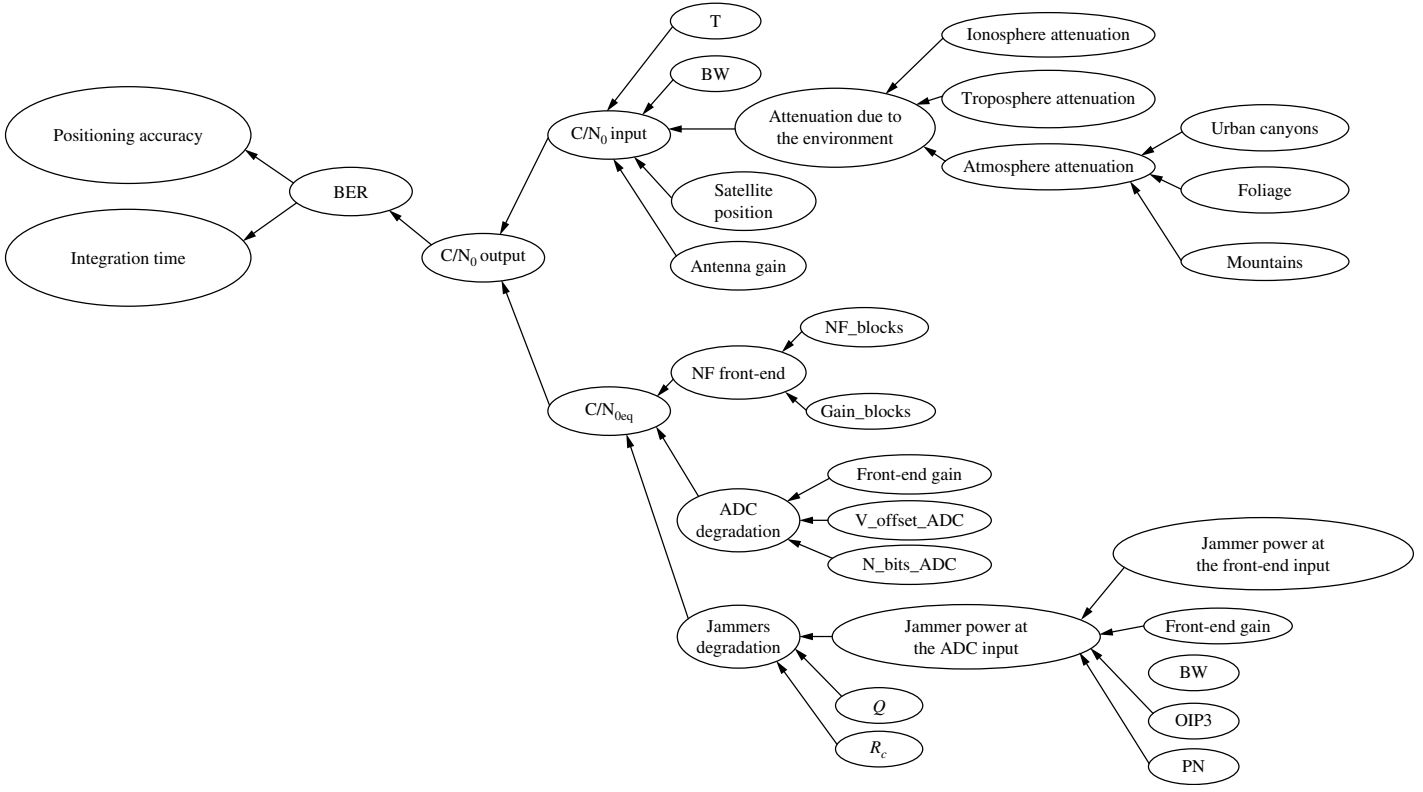

Figure 2-8 Relationship between various parameters of a GNSS receiver

performance quality of the front-end when it comes to the lowest signal power it can detect: the carrier-power-density-to-noise ratio (C/N_0), which is typically given in decibels.

The carrier-to-noise ratio (C/N_0) is related to the maximum bit error rate (BER) required for a GPS receiver at the output, which is 10^{-5} [Parkinson96]. Eq. 2-5 demonstrates that $C/N_0 f_d$ should be above 10 to achieve the necessary BER. If the navigation message has a frequency of 50bps, then the minimum required C/N_0 at the output of the RF front-end will be 27dB/Hz. On the other hand, thermal noise density at the input of the antenna is typically –174dBm/Hz and the minimum received input power in the case of GPS is –131dBm[ARINC00]. Therefore, C/N_0 at the input of the RF front-end results in 43dB/Hz. Thus, the maximum allowed noise figure can be obtained from the difference between the minimum expected C/N_0 at the input and the minimum required C/N_0 at the output, which comes out to 16dB.

Let's now move to the BOC (1,1)-modulated E1-L1-E2 Galileo signal. To ensure correct positioning for different receiver designs, the digital part of the receiver must have at least a C/N_0 of 30dB/Hz at the output of the RF front-end[Hein02]. Such a C/N_0 does not imply an error in the demodulation, it only means a higher or lower accuracy positioning. Figure 2-9 shows how RMS error in metres, due to code tracking error, increases exponentially for values of C/N_0 below 30dB/Hz. The thermal noise density at the input of the antenna is typically –174dBm/Hz and the minimum received signal power can be estimated as –128dBm.

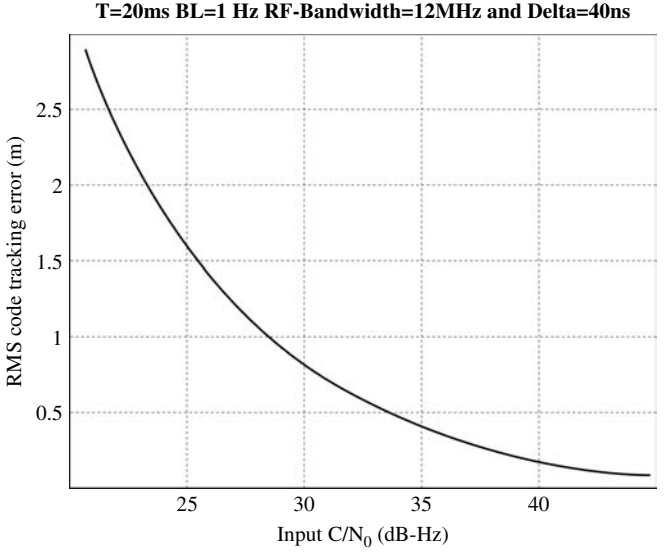

Figure 2-9 RMS code tracking error in metres

Therefore, the C/N_0 at the input of the RF front-end is 46dB/Hz. Thus, the maximum allowed noise figure (NF) for correct positioning can be set at 16dB. As was calculated for the GPS case, this is the difference between the minimum C/N_0 at the input and the minimum required C/N_0 at the output.

As the C/N_0 values employed for the calculations have been set to meet minimum requirements for a receiver the obtained NF values are the maximum ones allowed. However, not only the NF but also the integration time (T) of the receiver and the signal detection probability determine the quality of the receiver. For a better understanding of the relation among these parameters, an explanation of how a receiver acquires the signal is first required.

The signal acquisition process is a search process where it is necessary to repeat the C/A of the satellite from which the signal is received and the carrier frequency of the modulated code. The received carrier signal presents a frequency variation due to the Doppler Effect as a result of the speed of the satellite in its orbit and the speed of the receiver.

Figure 2-10 shows the bidimensional searching process. The generated C/A-code phase and the generated carrier frequency are swung, obtaining cells that are compared with the received signal by a correlation process. Every cell correlation process lasts T seconds. The decision to maintain or discard the signal is taken by comparing the value obtained in the correlation process with a given threshold value.

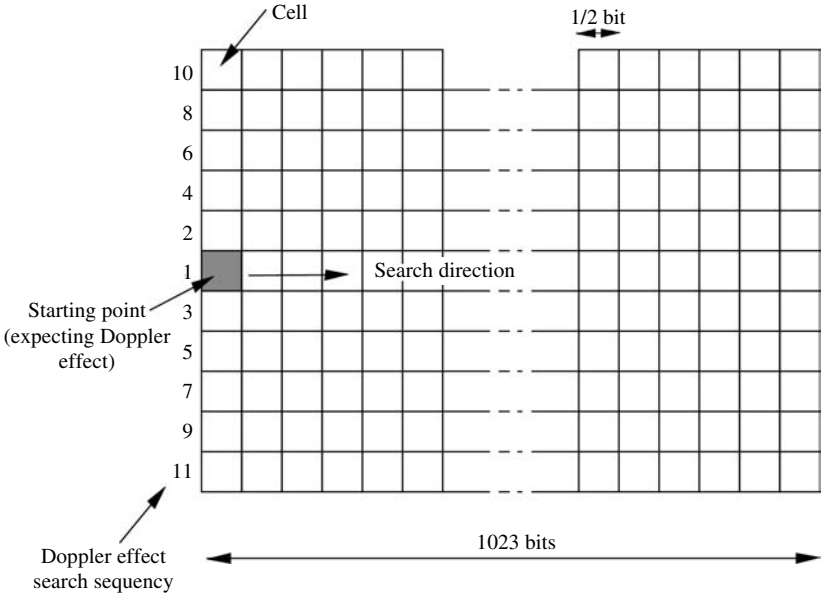

Figure 2-10 Bidimensional searching process

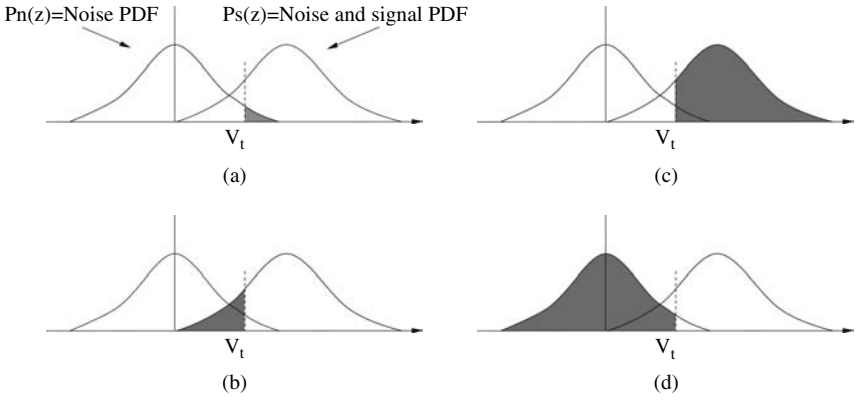

Figure 2-11 (a) False alarm probability. (b) False discard probability. Although there is a signal, it is not detected. (c) Signal detection probability. (d) Correct discard probability.

Every comparison has its probability density function (PDF); as there is noise with or without the signal in every cell, the detection process is a statistical one.

Figure 2-11 shows the probability density functions for the reception of the GPS L1 signal, when the decision is taken in the first try. If the obtained value is higher than a threshold value, the signal may be maintained; otherwise, it will be discarded. The signal detection probability $P_{d,}$ and the false alarm probability P_{fa}, when maintaining the signal is considered in its absence, can be analytically expressed by Eq. 2-6 and Eq. 2-7.

$$P_d = \int_{V_t}^{\infty} p_s(z)dz \tag{2-6}$$

$$P_{fa} = \int_{V_t}^{\infty} p_n(z)dz \tag{2-7}$$

where $p_s(z)$ is the probability density function in the presence of the signal, $p_n(z)$ is the probability density function in the absence of the signal, and V_t is a given threshold value.

As phase I and quadrature Q L1 signals are Gaussian distributed, probability density functions $p_s(z)$ and $p_n(z)$ can be calculated by Eq. 2-8 and Eq. 2-9[Kaplan96].

$$P_d = \frac{z}{\sigma_n^2} e^{-\left(\frac{z^2}{2\sigma_n^2} + \frac{s}{n}\right)} I_0\left(\frac{z\sqrt{2\,s/n}}{\sigma_n}\right) \tag{2-8}$$

$$P_d = \frac{z}{\sigma_n^2} e^{-\left(\frac{z^2}{2\sigma_n^2}\right)} \tag{2-9}$$

where:

- s/n is the signal-to-noise ratio estimated before signal detection ($10^{S/N/10}$).
- S/N is the signal-to-noise ratio estimated before signal detection in decibels and can be calculated by $C/N_0 + 10\log T$ (dB).
- T is the integration time for every cell before signal detection.
- σ_n is the root means square (RMS) noise power.

For threshold value $V_{t,}$ defined by Eq. 2-10 and a P_{fa} of 16 percent, the signal detection probability (P_d) can be calculated from Eq. 2-6 and Eq. 2-8. This results in Table 2-4, which shows P_d depending on C/N_0 and T for a normalised unity σ_n.

$$V_t = \sigma_n \sqrt{-21nP_{fa}} \tag{2-10}$$

The values in Table 2-4 can only be considered a guide as it takes commercial receivers more than one attempt to decide whether to maintain or leave a signal out . The values of the table have been shown here for a better understanding of the relation among the noise figure, signal detection probability, and integration time. Consequently, a proper noise figure can be obtained according to the features of the receiver.

As shown in Table 2-4, the higher C/N_0 is, the higher the signal detection probability will be, if it exists. This would, in turn, result in shorter integration time, which results in better receiver performance. This is why this process will require a lower noise figure than the previously defined maximum of 16dB, although it could sufficiently provide for accurate GPS or Galileo positioning.

TABLE 2-4 Detection probability versus C/ N_0 and integration time T

	C/N_0 (dB/Hz)			
P_d	$T = 0.001$ s	$T = 0.0025$ s	$T = 0.005$ s	$T = 0.010$ s
0.43105	30.00	26.02	23.01	20.00
0.63852	33.01	29.03	26.02	23.01
0.78084	34.77	30.79	27.78	24.77
0.87185	36.02	32.04	29.03	26.02
0.92721	36.99	33.01	30.00	26.99
0.95964	37.78	33.80	30.79	27.78
0.97807	38.45	34.47	31.46	28.45
0.98829	39.03	35.05	32.04	29.03
0.99384	39.54	35.56	32.55	29.54

Another reason for requiring a lower noise figure lies in the increasing use of GNSS receivers in urban environments. The received signal power is reduced in places with high buildings and narrow streets, reaching values of C/N_0 around 15dB/Hz in some cases. In this case, the receiver is unable to detect the satellite signal or provides an imprecise position. Moreover, another factor to consider in urban environments is the presence of interference signals that the receiver can capture, increasing SNR degradation.

A maximum noise figure of 3.5~4dB has been defined taking all these reasons into account. These values have been taken from an exhaustive study of commercial GPS receivers, making the receiver compatible with any detection method used today.

2.2.1.2 Linearity Receiver linearity requirements for GPS and Galileo receivers are not critical when it comes to the received signal because the power received is very low and practically constant. Linearity requirements are therefore imposed by receiver behaviour to external interferences. Section 2.2.2.3 shows a wider study of this behaviour.

2.2.1.3 Bandwidth As mentioned in section 2.1.3, the bandwidth of the Galileo signal is higher than that of the GPS signal. To be able to receive all the information sent, designers should choose the highest bandwidth. Nevertheless, lower bandwidth filters lower than those set by the standard can be applied without major damage to the C/N_0. Figure 2-12 shows the

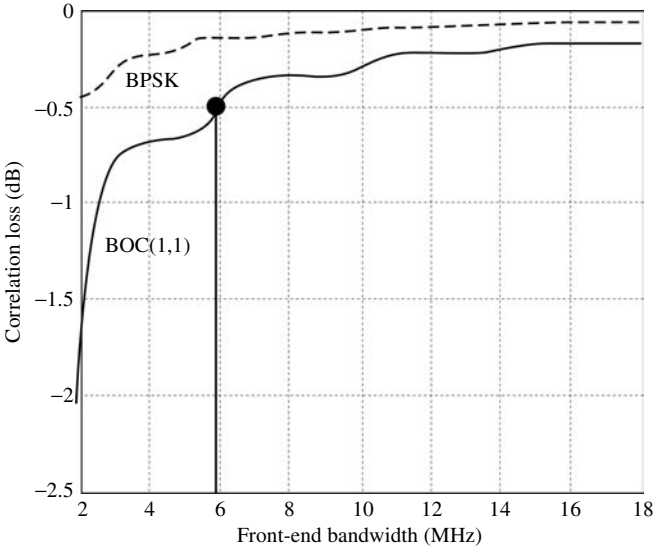

Figure 2-12 C/N_0 degradation versus receiver bandwidth

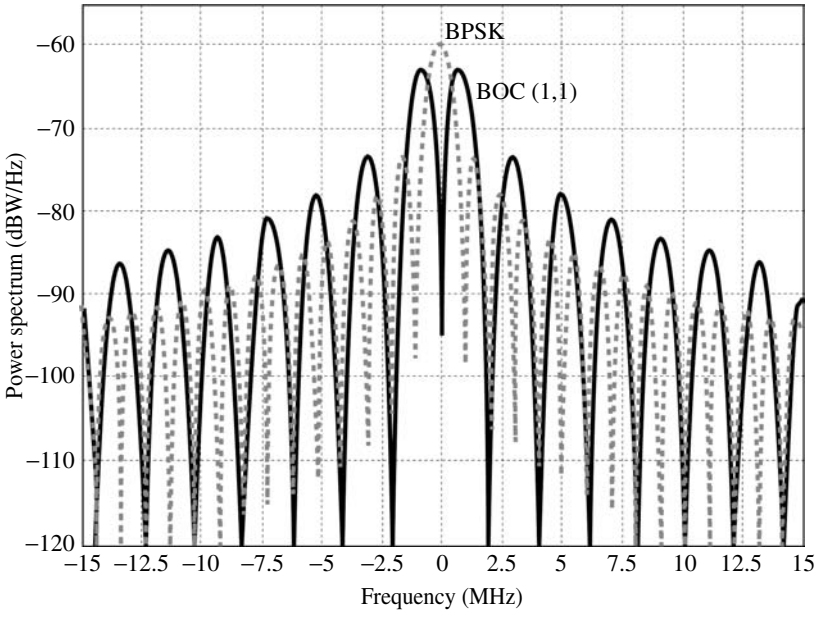

Figure 2-13 Power spectral density of a BOC (1,1) and BPSK-modulated signals

correlation loss due to the bandwidth of the filter used for signal reception. It can be seen that for a filter with a bandwidth higher than 14MHz, the degradation of C/N_0 is less than 0.25dB and losses increase exponentially for a filter with a bandwidth lower than 6MHz. Therefore, a 6MHz bandwidth is specified for the RF front-end to avoid degradation higher than 0.5dB and to be able to filter interferences in neighbour bands. It improves the C/N_0 ratio and sensitivity due to lower noise bandwidth.

Figure 2-13 shows that the specified bandwidth comprises the two main lobes of the Galileo BOC (1,1) signal as well as the main lobe of the GPS C/A-code with its two side lobes.

2.2.2 Receiver Specifications

Once the requirements of the receiver have been obtained, a number of important steps have to be carried out prior to starting with the receiver design. First of all, the gain, the C/N_0, and the linearity of the front-end have to be set to ensure proper performance of the receiver. Moreover, the receiver architecture has to be chosen and all the blocks and external components have to be specified to meet requirements.

2.2.2.1 Gain The required gain of the RF front-end is defined by the power at the input of the receiver chain and by the input analogue-to-digital

converter characteristics. The received input signal at the antenna has to be amplified until the ADC is able to digitalise it. Thus, the gain can be defined as the quotient of the input and output signal as expressed in the following equation.

$$G = \frac{\sigma_{N(\text{output})}}{\sigma_{N(\text{input})}} \tag{2-11}$$

where $\sigma_{N(\text{output})}$ is twice the maximum offset of the analogue-to-digital converter estimated to be 50mV [Baghai97] and $\sigma_{N(\text{input})}$ is the RMS value of the noise over 50Ω, which corresponds to –106dBm or 1.12μV (i.e., the threshold noise power at 290K in 6MHz). The system's voltage gain can now be obtained.

$$G = \frac{\sigma_{N(\text{output})}}{\sigma_{N(\text{input})}} = \frac{100\text{mV}}{1.12\mu\text{V}} = 91133 \tag{2-12}$$

Transforming the gain to decibels, it results in:

$$G[\text{dB}] = 20\log\left(\frac{\sigma_{N(\text{output})}}{\sigma_{N(\text{input})}}\right) = 99\text{dB} \tag{2-13}$$

The fact that the specified gain of 99dB is the minimum required gain for the detection of a signal of –130dBm must be kept in mind. If the gain were higher, lower power signals could be detected, thereby improving the sensitivity of the receiver. Moreover, there would be a surplus of the specified gain if the offset of the ADC were higher than the estimated 50mV. On the other hand, if the ADC had a lower offset, the system gain specification could also be decreased. However, this is usually not a contrasted value for the state-of-the-art technology when the time comes for system analysis.

Once it is defined, system gain should be shared among the blocks that compose the receiver. Before doing so, two critical points that determine final features of the receiver have to be taken into account. First, low-frequency amplifiers are more efficient than high-frequency amplifiers in terms of power consumption. Second, material in which the receiver is fabricated has to be able to isolate output and input in order to avoid oscillation problems caused by positive feedback. As an example, a substrate such as the SiGe process of AMS typically presents isolate levels at 1.6GHz below 40dB, while it is close to 90dB at the 3MHz isolation level. Therefore, splitting gain into different frequencies is required.

2.2.2.2 C/N_0 Degradation Due to the ADC Eq. 2-14 defines the C/N_0 without jamming in the baseband. This parameter is directly related to the

behaviour of the receiver under the probability of detecting the signal [Kaplan96].

$$C/N_0 = S_r + G_a - 10\log(kT_0) - NF - L \tag{2-14}$$

where S_r is the signal power at the input of the system in dBW, G_a is the antenna gain to the satellite in dBic, $10\log(kT_0)$ accounts for the thermal noise density in dBW/Hz, NF is the noise figure of the receiver, in dB and L considers the losses in implementation plus the ADC loss in dB. The degradation introduced by the digitalisation of a 1bit ADC can be obtained from [Chang82] and results in 2.2dB.

From the C/N_0 required for the system, the noise figure can be calculated by means of the Friis formula or system simulations for a given input signal power, antenna gain, receiver bandwidth, and 1bit ADC from Eq. 2-14. With this relationship, every component of the system can be characterised to make the whole system meet noise specifications.

2.2.2.3 Interferences Noise is usually defined as the floor of the lowest signal power that can be detected. On the other hand, linearity is defined as the ceiling of the highest signal power the system admits before saturation. The span between these two parameters defines the dynamic range of the receiver. Nevertheless, linearity definition should be slightly redefined in the case of GNSS signals because signal power is never high enough to saturate the system.

Even if the received signal is a low-power narrowband signal in the L1 band, signals from close bands, or even intermodulation products of other signals from other bands, could create a signal in the same band as the target signal. This is why linearity in the first blocks of the system is very important. Those signals will affect the performance of the signal processing, as they will not be filtered in the RF front-end. Therefore, the linearity of the GPS/Galileo receiver is redefined as the limit of the highest interference power that the receiver can handle before it begins to perform incorrectly.

As interferences are unwanted signals, they could be considered noise and therefore reduce the value of C/N_0 without distortion. In that case, the equivalent carrier-to-noise power density ratio (C/N_{0eq}) can be defined as in Eq. 2-15, where C/N_0 and J/S (the jammer-to-signal power ratio) are related to each other.

$$c/n_{0eq} = \frac{1}{\frac{1}{c/n_0} + \frac{j/s}{QR_c}} \tag{2-15}$$

where:

- c/n_0 is the carrier power-to-noise without jamming for a 1Hz band expressed as a ratio.
- j/s is the jammer-to-signal power ratio expressed as a ratio.
- R_c is the chipping rate of the GPS PRN code (chips/sec).
- Q is the spread spectrum processing gain adjustment factor (dimensionless).

To obtain the maximum allowed J/S for the receiver, the designer must set the minimum C/N_0 for an acceptable receiver (C/N_{0min}) and the specified C/N_0 for the receiver to be designed (C/N_0) which should be equal or lower than the previous one.

The difference between these two values will be the interference margin (M_{interf}), which is the allowed degradation in the C/N_0 due to interferences and can be calculated by Eq. 2-16.

$$M_{interf} = C/N_{0terminal} - C/N_{0min} \tag{2-16}$$

Nevertheless, interferences will not only degrade the C/N_0 but also quantification. Thus, even if it has a high enough C/N_0, the receiver may not work properly due to erroneous digitalisation. Therefore, depending on the quality of the ADC, the blocking level should be higher than the specified value in Eq. 2-16.

In the case of a 1bit ADC, due to the absence of a gain-controlled amplifier (GCA), interferences could cause the signal to cross the zero level in the input of the converter. In this case, the crossing would be generated by the unwanted interference rather than by a combination of random noise and the navigation signal. This would result in both erroneous digitalisation and incorrect localisation.

The maximum allowed degradation for the SNR in the 1bit quantifier by interference is 14dB M_{interf} (Eq. 2-16). This degradation is obtained when J/S is 32dB, which is achieved by an input power signal of –115dBm at the L1 and E1-L1-E2 band frequencies.

2.2.2.4 Architecture A multitude of well-known main RF front-end architectures are in existence: heterodyne, direct conversion, intermediate frequency digitalisation, and direct digitalization. For the combined GPS/Galileo front-end, a low-IF architecture can be selected. This architecture, when compared to Zero-IF, is insensitive to DC-offsets and flicker noise. The DC-offset compensation is a severe problem for Zero-IF receivers, as most of the GPS C/A-code signal energy comes

from DC. The main drawback of the low-IF architecture is its limited image rejection. This issue can be minimised when the frequency plan of the entire receiver is carefully designed. If the combined GPS/Galileo L1 signal is down-converted to a low IF of 20.42MHz, if the combined GPS/Galileo L1 signal is down-converted to a low IF of 20.42MHz, the rejection of the image signal by the RF SAW filter can be ensured. The obtained image rejection ratio can reach more than 40dB. By sampling the IF signal at 16.638MHz, the A/D converter also down-converts the incoming signal to a second IF of 4.092MHz. Signal detection is then performed digitally on a second chip that contains all the digital processing and controlling parts of the receiver. The PLL also allows the choosing of a LO frequency that down-converts the incoming RF signal directly to an IF of 4.092MHz. When this is chosen, the image that lies in the GPS/Galileo L1 band mainly consists of thermal noise. Choosing the gain level within the various blocks of the receiver is always a trade-off. A high-gain LNA will help reduce NF by minimising mixer contribution, but at the expense of higher power consumption in this block. A low-gain LNA may improve linearity and power consumption, but would require a low-noise mixer. Such a mixer would consume a lot of power. In other words, a low-gain LNA combined with a low-noise mixer may not offer a significant advantage in total power consumption over a high-gain LNA combined with a mixer with a higher NF. Therefore, a relatively high-gain receiver configuration has been chosen. Moreover, IF digitalisation requires few external components and is relatively simple. Thus, the front-end will consist of passive or active antenna, external filters, the LNA, the mixer, the PLL, amplifiers (RF and IF), and the ADC (see Figure 2-14).

Numerous applications can use a GPS/Galileo receiver. To add felxibility to the receiver, three different structures, both with and without an active antenna and the internal LNA have been studied. Figure 2-15 shows all three structures. Structure (A) makes use of an active antenna, avoiding the use of the LNA of the front-end. As the consumption of the LNA is not required, a very low-power front-end can be employed with a separated voltage supply for the LNA. The (B) and (C) structures employ the LNA and its antenna selection sensor, which sets the working mode of the LNA depending on the use of an active or passive antenna. The (B) structure makes use of an active antenna, which means the LNA is set to work in the low-gain mode so as not to saturate the system. Furthermore, higher sensitivity can be achieved by means of the gain of the external antenna. In the (C) structure, a passive antenna is employed and the LNA is set to the high-gain mode, avoiding the power consumption of the antenna and resulting in a low power consumption system.

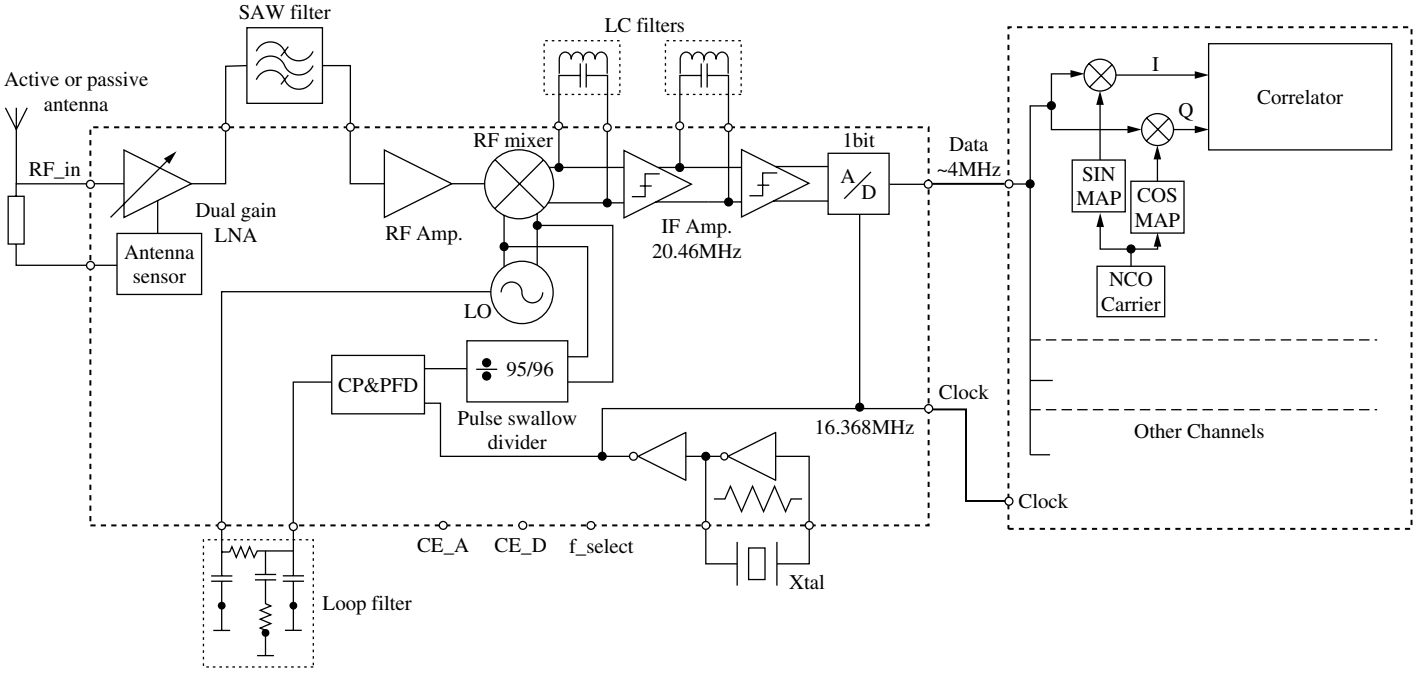

Figure 2-14 Block diagram of the receiver

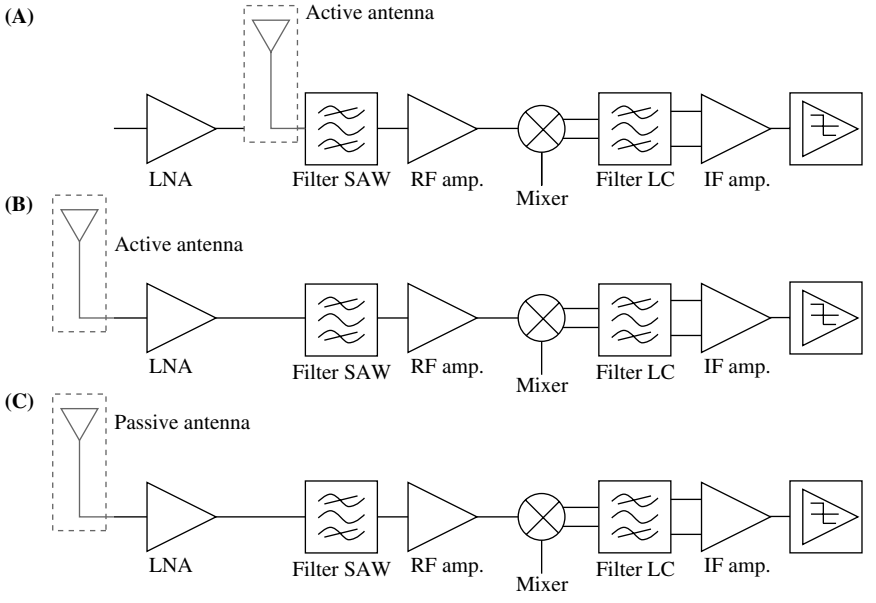

Figure 2-15 Receiver block diagram: (A) with active antenna and without the LNA; (B) with active antenna and the LNA; (C) with passive antenna and the LNA

2.2.2.5 Receiver Chain Specifications The specifications of the components of the proposed front-end are shown in Table 2-5. They have been obtained from the exhaustive system analysis of components and system simulations previously explained in this chapter. The supply voltage for the receiver has been defined as 3.3V, the operating temperature range as –30°C ~ +70°C, and the storage temperature as –40°C ~ +85°C.

From system simulations and analyses, gain, noise, linearity, and power consumption have been set to every component of the chain to meet required global specifications. Moreover, input and output impedances have been carefully selected to optimise the system gain and minimise the total noise. Due to the high gain required for the IF amplifier, two stages have been defined. If any change is required during the design stage, system simulations can be redone to reset the specifications for the blocks.

Front-end linearity is not an issue, since the received Galileo and GPS signals are low power and relatively constant. Therefore, the linearity specification is dictated by the required system's resistance to external interfering signals. The effects of the interferences on the three different structures previously mentioned have been studied for these specifications (see Table 2-5). They have been obtained from system simulations with a two-tone input. In these simulations, the minimum power that generates a third-order intermodulation product at the studied band

TABLE 2-5 Receiver chain specifications

Symbol	Parameter	Value	Unit
	LNA		
Gmax	High mode power gain	20	dB
Gmin	Low mode power gain	8	dB
NFmin	Noise Figure for Gmax	2.5	dB
NFmax	Noise Figure for Gmin	10	dB
OIP3	Output IP3	8	dBm
VSWRin	Voltage stat. wave ratio	<2	----
Power	Current consumption	7	mA
	RF amp.		
Gp	Power gain	17	dB
NF	Noise figure	5	dB
OIP3	Output IP3	5	dBm
VSWRin	Voltage stat. wave ratio	<2	----
Power	Current consumption	6	mA
	Mixer		
G	Voltage gain	6	dB
NF	Noise figure	17	dB
IIP3	Input IP3	–4	dBm
Zout	Output impedance	~1400	Ω
Power	Current consumption	7	mA
	IF_1 amp.		
G	Voltage gain	20	dB
IIP3	Input IP3	–15	dBm
Zin	Input impedance	~1400	Ω
Zout	Output impedance	~2400	Ω
Power	Current consumption	3	mA
	IF_2 amp.		
G	Voltage gain	>42	dB
OIP3	Output IP3	18	dBm
Zin	Input impedance	~1400	Ω
Zout	Output impedance	~2400	Ω
Power	Current consumption	3	mA
	Comparator		
Voffset—input	Input offset voltage	50	mV
Fc	Clock frequency	16.368	MHz
Power	Current consumption	<1	mA

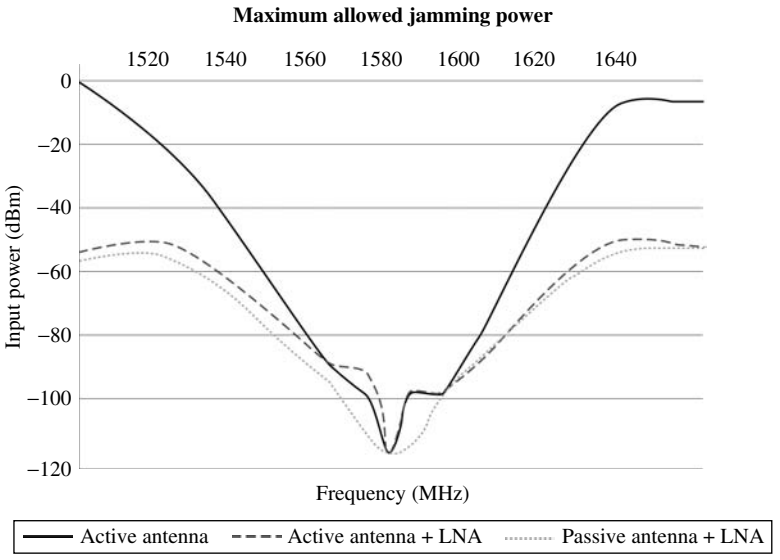

Figure 2-16 Interference blocking for the three receiver architectures under study

frequency of –115dBm has been obtained. Figure 2-16 shows maximum allowed power at the antenna input for interferences in the vicinity. This interference power corresponds with a J/S of 32dB at the L1 and E1-L1-E2 band frequencies. Then the maximum allowed degradation for the SNR in the 1bit quantifier by the interference can be obtained from Eq. 2-15 and Eq. 2-16 giving a $M_{int\,erf}$ of 14dB.

To quantify the interference blocking performance of the receiver an example is considered where the point at which the second harmonic of the result of mixing the signals of Inmarsat at 1645MHz and Iridium at 1610MHz reaches 1575MHz. Moreover, GPS antenna patterns experience attenuation when the elevation angle drops below 5°. The attenuation for the horizon line is typically around 15~20dB[Parkinson96]. Therefore, for a transmission power of 37dBm, the GPS/Galileo receiver can be located 50m from emissions without degrading receiver performance.

2.2.2.6 Frequency Synthesiser Specifications A frequency synthesiser, also known as a phase-locked loop (PLL), is a circuit that synchronises an output signal (generated by an oscillator) with an input reference signal to provide a stable and accurate signal frequency. This synchronisation is done in frequency as well as in phase. When both signals are synchronised, phase error is minimised. As in a control system, the output signal phase remains locked with the reference input signal phase.

Any oscillator signal shows instability in frequency and in amplitude. The target of an oscillator is to generate a signal with a fixed frequency. Frequency instability can be characterised through measurements of either frequency or time. In the time domain, the parameter used to measure instability is jitter noise, while phase noise is used to measure frequency. Moreover, frequency error should be below a certain level of parts per million (ppm). The main parameters used to gauge the performance of the synthesiser are phase noise, lateral band (spurious tones), and lock time. However, lock time is not a critical parameter for GPS/Galileo application due to the absence of different channels.

From the analysis of GPS front-ends, it has been observed that several models have digital outputs of 4.092MHz 1bit signals (i.e., [Atmel ATR0603], [Freescale MRFIC1505], [PHILIPS UAA1570HL], [SONY CXA1951AQ], and [ST STB5610]). This frequency is also suitable for the 6MHz bandwidth of the GPS/Galileo receiver. Therefore, a LO frequency of 1571.328MHz is required, which is mixed to the input frequency of 1575.42MHz. Crystal manufacturers offer a quartz crystal for GPS at a frequency of 16.368MHz. Moreover, this frequency is also employed as a clock for the GPS processor. On the other hand, to improve the frequency planning of the receiver, the down-conversion at the mixer is defined for an IF frequency of 20.42MHz. Therefore, a second LO frequency of 1554.96MHz is required. A 4.092MHz digital output is obtained by the ADC at a sampling frequency of 16.368MHz in the ADC. At the 20.42MHz IF frequency, the image signal is attenuated by the RF SAW filter and a higher rejection to the image signal is achieved. Moreover, mixer noise is also lower because it is filtered by the SAW filter. However, a bandpass filter at 20MHz has to be designed. At 4.092MHz, a low pass filter is sufficient, and efficiency of the IF amplifiers can be improved. Unfortunately, the noise and image signal are not filtered through the SAW filters. The frequencies involved in the PLL are summarized in Table 2-6.

A synthesiser based on integer-N architecture (see Figure 2-17) can be used to obtain the required output frequencies. The integer-N PLL has an output signal frequency N times the reference frequency, N being an integer. The output frequency can be changed by varying the value of N.

TABLE 2-6 Frequencies of the PLL

Fref	16.368MHz
Fout1	1554.96MHz
Fout2	1571.328MHz
ADCout	4.092MHz
IF1	20.42MHz
IF2	4.092MHz

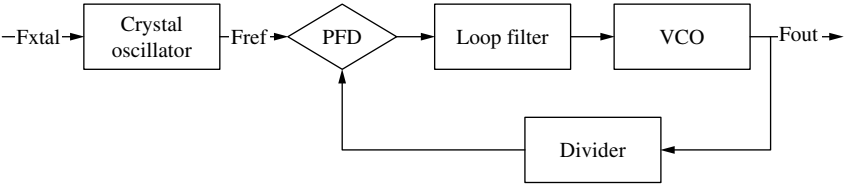

Figure 2-17 Integer-N PLL block diagram

N is 95 in the case of 1571.328MHz and 96 in the case of 1554.96MHz for the reference frequency of 16.368MHz.

The operation of the PLL is as follows: The output signal frequency is divided to compare it to the reference frequency in the phase frequency detector (PFD). Then the result is applied to a loop filter to obtain a control voltage for the VCO to lock the loop that is achieved when the output frequency is the desired one.

The operation conditions for the PLL have been defined by the system analysis. First, phase noise at the PLL has been defined. Three different zones can be distinguished regarding noise source. For frequencies close to the carrier, noise is generated by the crystal; approximately a decade away from the carrier, noise is contributed by PFD. The VCO is the main contributor to the total noise from a distance equal to the bandwidth of the PLL from the carrier frequency[Quemada07], [Simusyn].

The mask for the phase noise, taken from the analysis, is defined in Figure 2-18. Phase noise of [ST STB5610] has been taken at 1kHz from the carrier and phase noise of [Piazza98] at 100kHz.

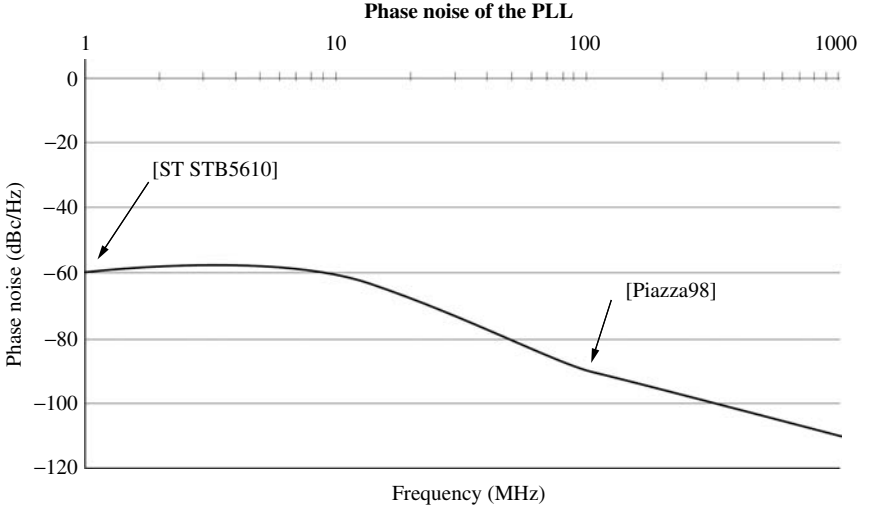

Figure 2-18 Phase noise mask

The gain of the VCO (K_{VCO}) is defined as the ratio between frequency and voltage variation. From the two working frequencies, 1554.960MHz and 1571.328MHz, a frequency range of ±0.5 percent is obtained. Component tolerance has to be taken into account as well. Inductor value depends only on geometric values, which is why measured integrated inductor tolerance is around ±1.5 percent[Aguilera03]. Thus, a characterisation of the inductors has to be done prior to the design. Capacitor tolerance is typically ±15 percent due to process variation and ±0.24 percent due to thermal variation[AMS]. Considering the resonance frequency shown in Eq. 2-17, the influence of the capacitor and inductor values on the frequency will be ±7.6 percent and ±0.75 percent, respectively.

$$f_{res} = \frac{1}{2\pi\sqrt{LC}} \tag{2-17}$$

Finally, a 1 percent safety margin has been defined to set a PLL specification for the output frequency range of around 10 percent (Eq. 2-18). Therefore, adding tolerance to the working frequencies, the VCO output signal has to oscillate between 1408MHz and 1717MHz.

$$\pm 0.5\% \pm 7.6\% \pm 0.75\% \pm 1\% \cong 10\% \tag{2-18}$$

Once frequency variation is obtained and control voltage is set between 0.5V and 2.8V, VCO gain equals 135MHz/V (Eq. 2-19).

$$K_{VCO} = \frac{\Delta f}{\Delta v} = \frac{1717 - 1408}{2.8 - 0.5} = 135 MHz/V \tag{2-19}$$

Basic specifications for the PLL are summarised in Table 2-7.

The Agilent ADS templates provide an environment to model PLL performance. *Open and Closed Loop Simulation of PLL* and *PLL_Noise Contribution* templates are used to characterise the PLL and analyse its noise, respectively.

TABLE 2-7 PLL specifications

2ndHarm	Spurious response, 2nd harmonic	<–23	dBc
PN	Phase noise@ 100kHz	<–90	dBc/Hz
Pout	Output power	0~3	dBm
Vcontrol	Control voltage	0.5–2.8	V
Current	Current consumption	<9	mA

TABLE 2-8 Input values for the *Open and Closed Loop Simulation of PLL* template of ADS

Fref	16.368MHz
Fout1	1554.96MHz
Fout2	1571.328MHz
K_{VCO}	135MHz/V
Kd	100μA
ω_p	40kHz

With the *Open and Closed Loop Simulation of PLL* template, a frequency response simulation can be carried out. Nevertheless, lineal models for the VCO, the divider, and the PFD are employed and no phase noise characteristics are considered. The input values for the simulation are shown in Table 2-8. K_{VCO} has already been defined in the previous section. Kd is the current of the charge pump and has been taken from the analysis and PLL simulations that set out to minimise it. Finally, the bandwidth, which is set by the loop filter, is chosen according to the highest value that fulfils the noise and PLL specifications. The absence of different channels in the application offers freedom to choose the loop bandwidth value. The higher it is, the more time it requires to lock the loop and the lower the noise at the output. The bandwidth is set by the loop filter and has an influence on the output noise[Quemada07].

The band attenuation and loop filter components that meet the requirements are obtained from the simulations. The phase margin should be between 30º and 70º as stated in[Wolaver 91]. For a phase margin around 50º, an attenuation of 29/30dB and a bandwidth of 40kHz are obtained. The values of the third-order loop filter (see Figure 2-19) have been obtained from these results and are shown in Table 2-9.

Figure 2-20 shows the VCO phase noise contributors and phase noise mask obtained by the *PLL_Noise Contribution* template for the previously set values. As explained, for frequencies close to the carrier,

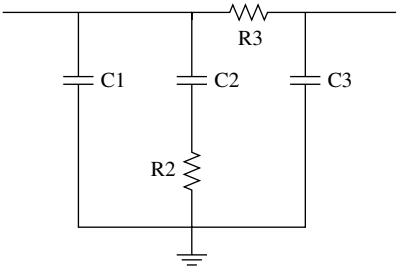

Figure 2-19 Loop filter circuit scheme

TABLE 2-9 Loop filter values

Component	Value	Unit
C1	659	pF
C2	3.27	nF
C3	65	pF
R2	3.141	kΩ
R3	813	Ω

noise is generated by the crystal. Approximately a decade from the carrier, noise is contributed by PFD from a distance equal to the bandwidth of the PLL from the carrier frequency; the VCO is the main contributor to the total noise[Quemada07]. It can be seen that phase noise requirements can be fulfilled, accomplishing the previously defined set of design specifications.

2.3 Summary

The front-end has been specified in order to work simultaneously with GPS and Galileo. This has been made possible by a study of the two standards, and the analysis of their requirements and system simulations. Therefore, the next objective, the design of the front-end, can be undertaken.

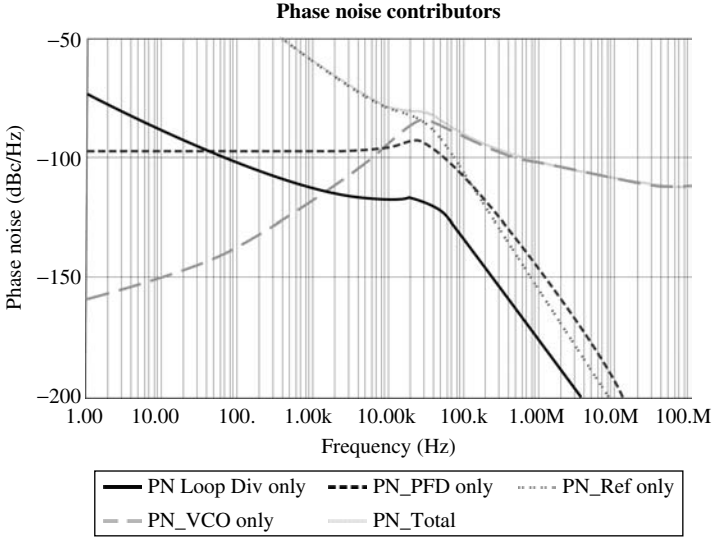

Figure 2-20 PLL_Noise Contribution template results for the PLL phase noise

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Chapter

3

Circuit Design

Considering the technical requirements defined in the previous chapter as the starting point, this chapter will explain in detail the design of every block of the radio frequency (RF) front-end. To accomplish a design that fulfils specifications, the design is verified by means of the electrical schematic simulations, layout of the different components of the electrical schematic and post-layout simulations considering additional effects introduced by tracks, pads, such as stray capacitances , stray resistances carried out by RF engineers. Circuit design considerations, as well as the results of post-layout simulations for all the blocks of the front-end, are presented in this chapter. The receiver chain and the phase-locked loop (PLL) are described separately. Moreover, the control logic, the PADs, and the floor planning of the RFIC are also presented. The design has been fabricated with a 0.35μm SiGe process, with four metal layers, two polysilicon layers, and a high-resistivity polysilicon layer (AMS-SiGe 0.35μm-BYS) to reduce both cost and power consumption.

3.1 Receiver Architecture

Figure 3-1 shows the proposed low-IF architecture for the combined GPS/Galileo front-end, which is explained in greater detail in Chapter 2. This architecture, compared to Zero-IF, is insensitive to DC offsets and flicker noise. In Zero-IF receivers, DC-offset compensation is a severe problem since most GPS C/A-code signal energy is DC. The main drawback of a low-IF architecture is its limited image rejection. This can be improved when the frequency plan of the entire receiver is carefully designed. In the implemented receiver, the combined GPS/Galileo L1 band signal is down-converted to a low IF of 20.42MHz, causing the image signal to be rejected by the RF SAW filter. The obtained image

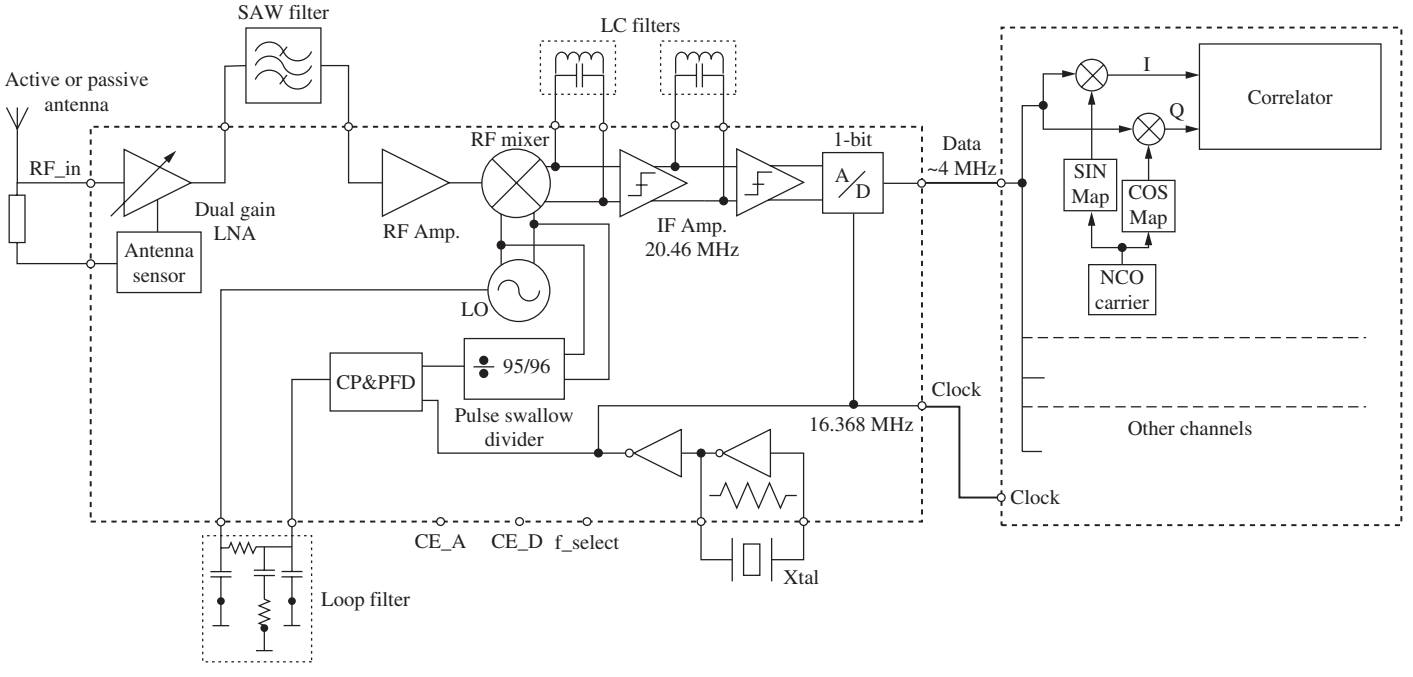


Figure 3-1 Block diagram of receiver

rejection ratio is more than 40dB. When sampling the IF signal at 16.638MHz, the A/D converter also down-converts the incoming signal to a second IF of 4.092MHz. Signal detection is then performed digitally on a second chip that contains all the digital processing and controlling parts of the receiver.

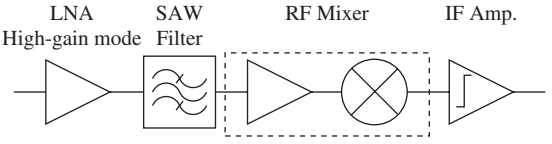
The PLL also allows for the choice of an LO frequency that down-converts the incoming RF signal directly to an IF of 4.092MHz. For this choice, the image lies in the GPS/Galileo L1 band and mainly consists of thermal noise.

Choosing the gain of the various blocks of the receiver is always a trade-off. A high-gain low-noise amplifier (LNA) will help to reduce Noise Figure (NF) by minimising mixer contribution, but at the expense of higher power consumption in this block. A low-gain LNA may improve linearity and power consumption, but would require a low-noise mixer. Such a mixer would consume a great deal of power. In other words, a low-gain LNA combined with a low-noise mixer may not offer a significant advantage in total power consumption over a high-gain LNA combined with a mixer with higher NF. Therefore, as shown in the previous chapter, a relatively high-gain receiver configuration has been chosen. Figure 3-2 shows the resulting receiver specifications with gains, NF, and IIP3 given below each block. Front-end linearity is not an issue, since the received Galileo and GPS signals are very low power and relatively constant. Therefore, linearity specifications are dictated by the required system's ability to perform in the presence of external interfering signals.

The total SSB noise figure, referring to the input of the on chip LNA, is 2.8dB, which is adequate for high-sensitivity applications.

The front-end bandwidth is approximately 6MHz, which comprises the two main lobes of the Galileo BOC(1,1) signal as well as the main lobe of the GPS C/A-code with its two side lobes. The C/N_0 correlation loss caused by front-end filtering is less than 0.7dB for both signals.

Finally, the second IF signal is converted to digital signal with a 1bit A/D converter. Using a 1bit converter results in slightly degraded



	LNA High-gain mode	SAW Filter	RF Mixer	IF Amp.
Gain	20dB	–3.5dB	23dB	> 55dB
NF	2.5dB	3.5dB	6.5dB	-----
IIP3	–16dBm	-----	–23dBm	-----

Figure 3-2 Receiver specifications

performance compared to that of multibit converter, but it allows the design of a simpler, lower-power receiver without automatic gain control.

3.2 Low-Noise Amplifier

A dual-mode LNA with an integrated antenna sensor has been designed. The two LNA modes are comprised of a high-gain mode for a passive antenna and a low-gain mode for an active antenna, enabling the receiver to sense the presence of a passive or active antenna and avoid the risk of early receiver overloading due to unwanted interference signals.

As shown in Figure 3-3, the low-noise amplifier consists of three subsystems: the core of the LNA, the antenna sensor circuit, and the gain selection stage.

3.2.1 LNA Core

The aim of the LNA is to amplify the low-power input signal received by the antenna while degrading the C/N_0 as little as possible. Providing an input and output impedance of 50Ω is also a critical requirement of the LNA. In the case of the input impedance, it serves as a way to match the antenna impedance, where, in the case of the output impedance, it helps to avoid an undesired degradation of preceding SAW filter characteristics (insertion loss, pass band ripple, etc.) due to mismatched impedances.

The 50Ω input impedance can be achieved by adding an inductance in series with the emitter of the input transistor to degenerate the common emitter amplifier, as shown in Figure 3-4. This is the most popular LNA

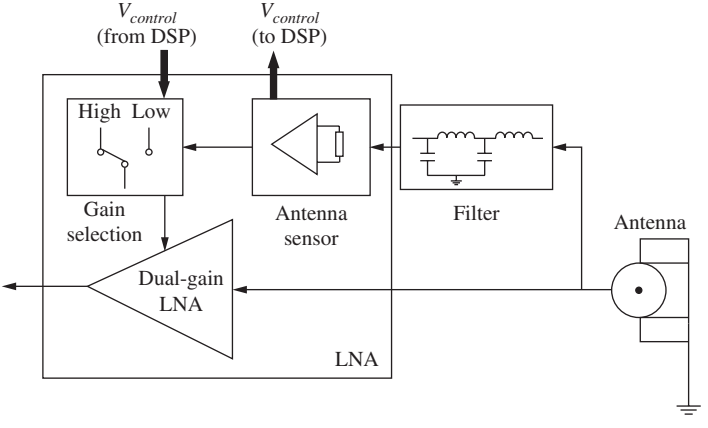


Figure 3-3 LNA building blocks

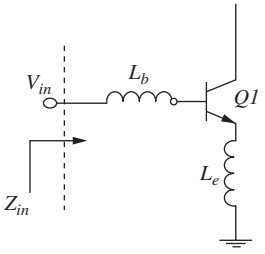


Figure 3-4 Common emitter amplifier with emitter degeneration

topology because it simultaneously achieves low-noise, high-gain, and input impedance matching compatible with a narrow frequency band.

Figure 3-5 shows the small signal equivalent circuit of the input transistor. Excluding the base-collector capacitance, the base emitter, and the emitter resistors, the input impedance of the amplifier can be illustrated as shown in Eq. 3-1.

$$Z_{in} = r_b + s(L_b + L_e) + \frac{1}{sC_{be}} + \left(\frac{g_m}{C_{be}}\right)L_e \tag{3-1}$$

It should be noted that there is a resistive component in the input impedance. To reach a resistive input impedance of 50Ω at the operating frequency, one can choose the value of L_b and L_e such that C_{be} is resonated at the operating frequency with $(g_m/C_{be})L_e+r_b$ equal to 50Ω. Eq. 3-2 and Eq. 3-3 are then solved, resulting in an input impedance of 50Ω.

$$j\omega_0(L_b + L_e) + \frac{1}{j\omega_0 C_{be}} = 0 \tag{3-2}$$

$$\left(\frac{g_m}{C_{be}}\right)L_e + r_b \approx \omega_T L_e + r_b = 50\Omega \tag{3-3}$$

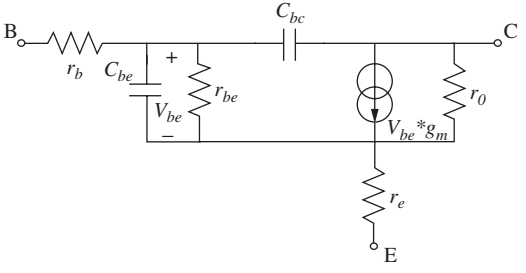


Figure 3-5 Small equivalent circuit of the SiGe input transistor

One of the most appealing advantages of this topology is that most of the resistive components of the input impedance are noiseless because they are synthesised with an inductor, unlike other techniques where a noisy resistor is added to the signal path to provide 50Ω termination resistance[Shaeffer97]. This explains the low-noise performance and popularity of the inductively degenerated common emitter LNA.

When calculating the effective small-signal transconductance of the input transistor, it is worth noticing that the input-matching circuit is a pure series RLC resonant circuit. At resonance, the voltage across is enhanced by Q amount of times, where Q is the quality factor of the input-matching RLC network. In other words, the Q enhancement mechanism provides a free gain of Q for both the input signal and the noise from the source resistance R_S. The added gain from the input-matching circuit helps to mitigate the effect of the channel's thermal noise, which accounts for the superior noise performance of the common-source LNA with inductive degeneration. Furthermore, the effective transconductance is also enhanced by a factor of Q as shown in Eq. 3-4[Li04]:

$$G_m = g_m Q = \frac{g_m}{\omega_0 C_{be}(R_s + \omega_T L_e)} = \frac{\omega_T}{\omega_0 R_s \left(1 + \frac{\omega_T L_e}{R_s}\right)} \tag{3-4}$$

If the input is matched to R_s as shown in Eq. 3-5, transconductance results in:

$$G_m = \frac{1}{2R_s}\frac{\omega_T}{\omega_0} \tag{3-5}$$

R_s is usually equal to 50Ω in an RF system. It is worth noting that the effective transconductance G_m is only related to the ratio of ω_T to ω_0 and is not dependent on small-signal transconductance g_m. However, parasitic input path capacitance and base-collector capacitance are also present. The base-collector capacitance C_{bc} provides a feedthrough path from input to output and thus decreases the reverse isolation. In addition, its interaction with the inductive load at the output introduces a negative resistance at the input, which causes stability concerns. Furthermore, the Miller effect of C_{bc}, and the C_p associated with the bond pad provides a shunt current branch at the input, which further complicates input matching. One can add a cascade stage to mitigate the Miller effect of C_{bc} and improve the reverse isolation. However, this results in additional noise from the cascode transistor, which degrades the noise figure if not optimally designed[Li04].

The core of the implemented cascoded LNA with the resistor chain [Fong99][García01] (used to perform gain switching) is shown in Figure 3-6. Transistors *Q1* and *Q2* and degeneration on-chip inductors L_e (900pH) form the previously mentioned common emitter transconductance stage[Shaeffer97]. These transistors have multiple-base

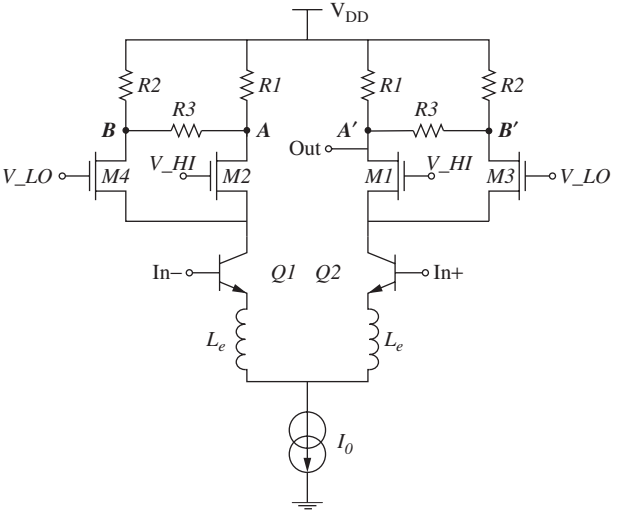


Figure 3-6 LNA core

contacts in order to minimise the noise introduced by the base resistance r_b, thereby reducing the NF (Eq. 3-6).

$$NF = 1 + \frac{r_b}{R_S} + \frac{V_T}{2 \cdot R_S \cdot I_C} + \frac{I_C \cdot R_S}{2 \cdot V_T \cdot \beta} \tag{3-6}$$

where R_s is the source resistance and I_C is the collector current. Base shot noise is not included in Eq. 3-6 as a current noise source[Razavi97]. As mentioned before, the degenerating inductors allow conjugate input impedance matching and improve circuit linearity.

As the RF input signal is single-ended (In+), In– is consequently grounded through a 22pF capacitor. The use of a single-ended input within a differential-like architecture reduces the number of external components (such as a balun) and mitigates the effect of parasitic ground and V_{DD} bondwire parasitics on LNA performance. The amplified RF current, by means of *Q1* and *Q2* transistors, flows through both *M1* and *M2* cascode transistors to reach the LNA output in high-gain mode. In low-gain mode, the amplified RF current flows through both *M3* and *M4* cascode transistors before being split by resistor chains (*R1* and *R2*), while *M1* and *M2* are switched off during the gain-switching stage. The gain step between the two modes of operations depends (during initial approximation) on the resistor ratio *R2*:*R1*. The advantage of this kind of configuration is that the gain step does not depend on how accurately the resistors match in terms of their absolute value, but on their ratio *R2*:*R1*. Therefore, the gain step can be accurately controlled.

In the high-gain mode, the gate voltage of the transistors is set to the appropriate values to switch on *M1* and *M2* and switch off *M3* and *M4*. Hence, both transistors *M1* and *M2* act as cascode transistors in the

transconductance stage. LNA gain is the highest in this mode because the amplified RF current is injected into nodes *A* and *A'*, which have the highest resistance of the resistor chains.

In low-gain mode, *M3* and *M4* act as cascode transistors while *M1* and *M2* remain switched off. The LNA gain is the lowest because the current from the transconductance stage is injected into nodes *B* and *B'*, which have the lowest resistance of the resistor chain.

An emitter follower stage is used at the LNA output to perform on-chip output impedance matching. It also contributes to the system input/output isolation, therefore improving amplifier stability.

3.2.2 Antenna Sensor and Gain Selection Circuitry

In order to select high gain (for passive antennas) or low gain (for active antennas) for the LNA, the system is able to detect automatically whether the antenna is active or passive by means of the antenna sensor (see Figure 3-7)

The antenna sensor detects the antenna type and sets the *AS_OUT* pin as shown in Table 3-1.

The operation of the sensor is very simple and can be explained in two steps:

- An active antenna consumes a current that flows through R_{ant}. It will generate a voltage difference between R_{ant} and the *AS_OUT* pin will be "high."
- A passive antenna does not consume any current, so there is not a voltage difference at R_{ant}, resulting in the *AS_OUT* pin being "low."

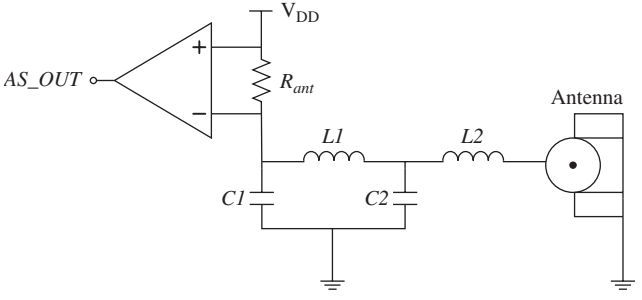


Figure 3-7 Antenna sensor circuit

TABLE 3-1 ***AS_OUT*** **pin, antenna sensor**

Antenna Type	*AS_OUT* Logic Value
passive	low
active	high

The control signal *AS_OUT* is buffered out to the digital control with information about the antenna type, which allows the digital processing unit (along with information about the C/N_0) to establish the gain requirement. The digital processing unit then sets the control voltage *GC* back to the gain selection stage of the LNA.

The gain selection circuit (see Figure 3-8) sets the bias voltage, controlled by the *GC* pin (see Table 3-2), to make the LNA work in high-gain or low-gain mode.

The values of the *V_HI* and *V_LO* nodes set the gain of the LNA by changing the bias voltage of the core's cascode transistors. The ON and OFF voltages have been defined as 3.3V and 1.1V, respectively. In high-gain mode, the *GC* will be low and *M1* will be ON and *M2* OFF, establishing 3.3V for *V_HI* and 1.1V for *V_LO,* set by the voltage difference at *R1*.

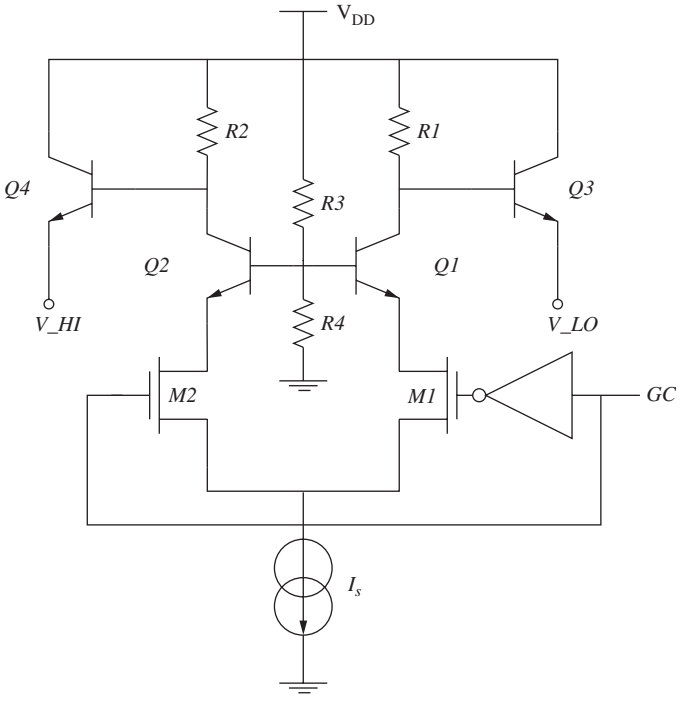


Figure 3-8 Gain selection circuit

TABLE 3-2 Gain selection by means of the Gain Control (GC) pin states

GC Logic Value	Gain
low	max
high	min

3.2.3 Layout Considerations and Simulation Results

Figure 3-9 shows a microphotograph of the designed dual-gain LNA. The emitter-degenerating inductances, the power supply decoupling capacitors, and the amplifier connection pads can be clearly identified.

The V_{DD} decoupling capacitors filter out any bias noise and help improve LNA stability, which is of concern due to capacitive and bondwire coupling between the bias voltage and RF input/output pins. RF pads rely solely on the top thick layer of metal to minimise parasitic capacitance. The size of the LNA's chip (including decoupling capacitors and pads) is $1\times1.5\text{mm}^2$.

V_{DD} and GND pads are double, allowing two bondwires to reduce their parasitic inductance. Therefore, AC ground and supply loops resulting from bondwire and package parasitic inductances are less significant, reducing the risk of undesired oscillations.

To analyse realistic situations through simulation, different parasitic effects must be taken into account. To obtain realistic results, the simulation setup includes the effects of PAD parasitic capacitances, bondwire inductances, bondwire coupling between different pins, and package parasitics, among others.

The block requirements reported in the previous chapter and post-layout simulation results of the LNA are shown in Table 3-3.

Due to the strict specifications previously set, the performance of the receiver will not be seriously affected by the fact that the gain and noise figure of the LNA are slightly worse than specified. Moreover, the gain of other front-end blocks will be increased to compensate for the lower gain in this stage. In addition, as the noise figure is slightly higher, a marginally worse performance of the receiver will be expected in regards to the C/N_0.

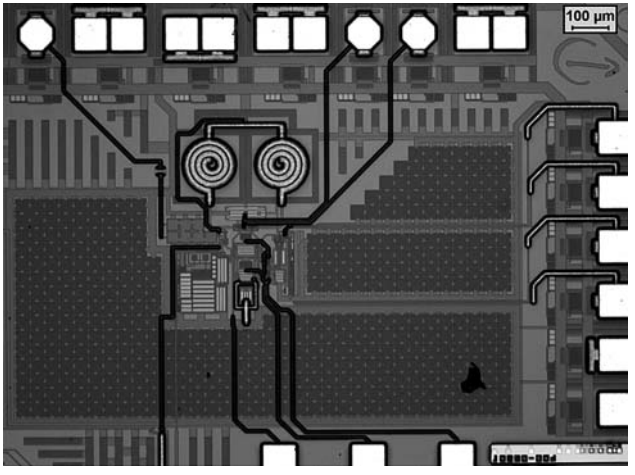


Figure 3-9 LNA microphotograph

TABLE 3-3 Post-layout results

	Specifications		Post-layout		
Parameter	**Gmin**	**Gmax**	**Gmin**	**Gmax**	**Unit**
S11	< –10		–18.2	–14	dB
S22	< –10		–7.6	–21.8	dB
Gain	20	8	19.7	9	dB
NF	2.5	10	2.8	10.8	dB
Current	<7		7.5		mA

3.3 RF Pre-Amplifier and Mixer

To obtain the required gain and noise figure in the down-conversion stage, an RF preamplifier has been implemented before the mixer. The following subsections describe and present the design and combined performance of both blocks (pre-amplifier and mixer).

3.3.1 RF Pre-Amplifier

The input signal of the RF amplifier comes from an external SAW filter, so the input impedance must be 50Ω to maximise transferred power and not degrade SAW filter performance due to mismatched impedance.

Even though the RF amplifier input signal is single-ended, a differential structure has been selected based on its advantages (see Table 3-4).

The inductive degeneration common emitter differential amplifier shown in Figure 3-10 has been chosen to maximise the gain and minimise the noise figure and power consumption.

3.3.2 Mixer

An active mixer has been selected because it presents a higher gain and lower noise than the passive ones. Gilbert mixers are the most widely used active mixers. This mixer is formed by two different stages[Gilbert68]: the amplification stage and the mixing core (see Figure 3-11). In the

TABLE 3-4 Advantages and disadvantages of a differential stage

Advantages	Disadvantages
■ Rejection to common mode noise coupled through the substrate.	■ A balun is needed to transform the single-ended signal coming from the antenna to the differential. This adds extra signal losses, degrading NF.
■ Effect of package parasitics is reduced.	■ The number of components is increased.
■ The chip's ground plane quality is improved.	■ Power consumption is higher for the same gain and NF.

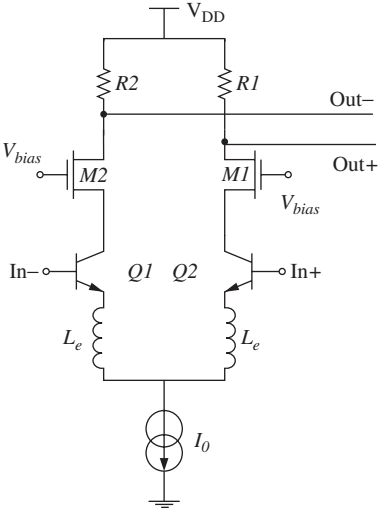


Figure 3-10 RF pre-amplifier with emitter degeneration

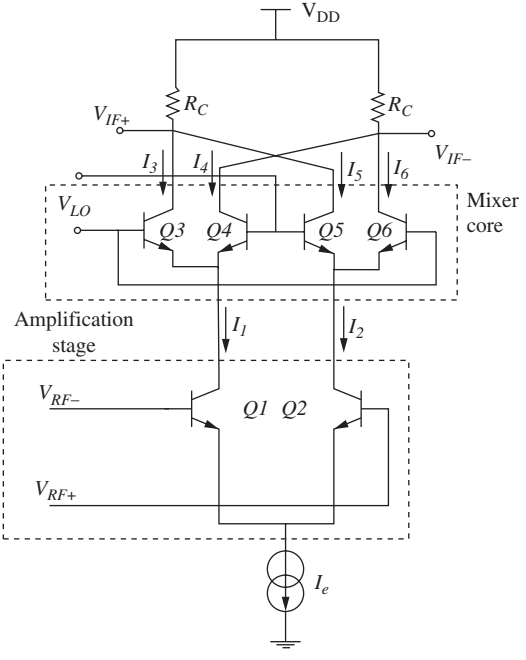


Figure 3-11 Gilbert cell

figure, V_{LO} is the local oscillator voltage input signal, V_{RF} is the radio frequency voltage input signal, R_c is the collector resistance, V_{DD} is the voltage supply, V_{IF} is the intermediate frequency voltage output signal, and I_e is the bias current.

In the following subsections, the mixer's performance is expressed as a function of a number of individual components (collector resistance R_C, transistor size, number of base contacts, bias current of the mixer I_e, etc.). Mixer design guidelines have been taken from equations of behavioural models and from the authors' previous experience in mixer design[Rodriguez05].

3.3.2.1 Conversion Gain in Gilbert Mixers The conversion gain value is obtained by multiplying two voltage signals. On the one hand, the well-known output voltage (V_{od}) of the input differential pair [Gray84] is as follows:

$$V_{od} = \alpha_F I_e R_C \tanh\left(\frac{V_{RF}^{-} - V_{RF}^{+}}{2V_T}\right) = 2I_C R_C \tanh\left(\frac{-V_{RF}}{2V_T}\right) \qquad (3\text{-}7)$$

where I_C is the collector current, V_{RF} is the input voltage, and V_T is the thermal voltage. In Eq. 3-7, when RF is a small signal (V_{RF} <<), the hyperbolic tangent of x can be approximated by x, yielding:

$$V_{od} = 2I_C R_C \left(\frac{-V_{RF}}{2V_T}\right) \qquad (3\text{-}8)$$

On the other hand, a square local oscillator (LO) signal can be approximated with the first term of a Taylor series:

$$V_{LO} = \frac{2}{\pi} \qquad (3\text{-}9)$$

The voltage gain (G_v) can be obtained by multiplying Eq. 3-8 and Eq. 3-9. When LO switches are driving current, the collector resistor for the amplification stage is R_C (in Figure 3-11) and r_e of transistors in the amplification stage. Normally, as r_e is much smaller than R_C ($r_e << R_C$), r_e is not included in Eq. 3-10.

$$\frac{V_{IF}}{V_{RF}} = G_V = -R_C g_{mRF} \frac{2}{\pi} \qquad (3\text{-}10)$$

where G_v is the voltage conversion gain, R_C is the collector resistance, and g_{mRF} is the transconductance of the transistors in the amplification stage.

As can be seen in Eq. 3-10, the following is necessary to increase gain:

- The transconductance of transistors in the amplification stage g_{mRF} should be as high as possible. This parameter is directly influenced by bias current I_e.
- Collector resistance R_C should be as high as possible. The limit of this resistor value depends on the output frequency because of the trade-off between gain and bandwidth.

3.3.2.2 Noise Figure in Gilbert Mixers The main contributor to the noise figure in Gilbert mixers is the amplification stage, due to the fact that the signal has already been amplified afterwards and, applying Friis equation [Lee98], the noise added to the signal after amplification has less importance. To get an idea of the amount of noise added in this stage, each transistor in the differential pair is substituted for its quasi-linear noise model [Xavier97], which can be used at frequencies below 6GHz (see Figure 3-12).

In Figure 3-12, resistances (R_s, r_b, r_e, and r_c) generate thermal noise shown in Eq. 3-11:

$$v_{nr}^2 = 4\mathrm{kT}r \tag{3-11}$$

where k is Boltzmann´s constant, T is temperature, and r is the resistance value (Ω).

Base and collector currents (I_b and I_c) generate shot noise shown in Eq. 3-12:

$$i_{nb}^2 = \frac{2\mathrm{kT}g_m}{\beta} \qquad i_{nc}^2 = 2\mathrm{kT}g_m \tag{3-12}$$

where g_m is the heterojunction bipolar transistor (HBT) transconductance.

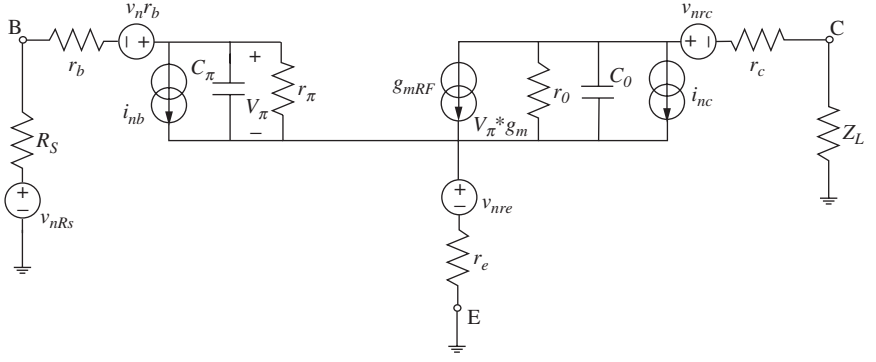


Figure 3-12 Hybrid π noise model

Base current (I_b) also generates flicker noise:

$$i_{nf}^2 = \frac{2q\, I_b\, f_1}{f} \tag{3-13}$$

where q is the electronic charge and equals to 1.6×10^{-19}, f_1 is the corner frequency and f is the frequency of interest. The flicker noise defined by Eq. 3-13 becomes dominant at frequencies below the corner, f_1 value, and can be neglected above a few kilohertz.

As can be seen in Figure 3-12, noise generators must be added: two current sources that represent the shot noise of the collector and base currents, and four voltage sources that represent the noise generated by the source resistance (R_s), parasitic base, emitter, and collector resistances (r_b, r_e, and r_c, respectively). Transferring all these sources to the input yields the model shown in Figure 3-13.

In Figure 3-13, v_{ns} is the noise generated within the source and v_{nm} is the noise of the mixer converted to a voltage source at the input. The different noise sources included in v_{nm} are shown in Eq. 3-14:

$$v_{nm}^2 = v_{nr}^2 + v_{nb}^2 + v_{nc}^2 \tag{3-14}$$

where v_{nr} is the thermal noise of parasitic resistances, v_{nb} is the base-emitter shot noise, and v_{nc} is the collector emitter shot noise.

Thermal noise of parasitic base and emitter resistances is shown in Eq. 3-15:

$$v_{nr}^2 = 4\mathrm{kT}(r_b + r_e) \tag{3-15}$$

The thermal noise of the collector resistor is disregarded because the noise of r_c is typically 10^5 times lower than collector-emitter shot noise [Xavier97].

Base-emitter shot noise is converted to a voltage noise source in series with the source resistor by applying the Thevenin conversion as shown in Eq. 3-16:

$$v_{nb}^2 = \frac{2\mathrm{KT}\, g_m (r_b + r_e + Z_n)^2}{\beta} \tag{3-16}$$

where Z_n is the base impedance.

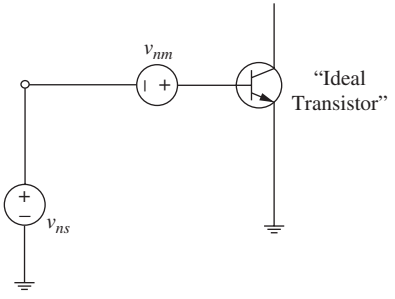


Figure 3-13 Noise model of transistor

The voltage source associated to the collector-emitter shot noise is shown in Eq. 3-17:

$$v_{nc}^2 = \frac{2\mathrm{KT}}{g_m}\left(1 + \frac{(r_b + r_e + Z_n)^2}{Z_{be}^2}\right) \tag{3-17}$$

where Z_{be} is the parallel of r_π and c_π in Figure 3-12.

The noise figure expression of a device can be derived from the ratio between the total noise at the output to the noise of the source as shown in Eq. 3-18:

$$NF = \frac{Gv_{ns}^2 + Gv_{nm}^2}{Gv_{ns}^2} = \frac{v_{ns}^2 + v_{nm}^2}{v_{ns}^2} = 1 + \frac{v_{nm}^2}{v_{ns}^2} \tag{3-18}$$

where v_{ns} is the noise at the input of the device and v_{nm} is the noise of the device itself.

The noise figure expression is obtained by substituting Eq. 3-15, Eq. 3-16, and Eq. 3-17 in Eq. 3-14 and the last part of Eq. 3-8:

$$NF = 1 + \frac{r_b + r_e}{\mathrm{Re}(Z_n(t))} + \frac{1}{2g_m(t)\,\mathrm{Re}(Z_n(t))} + \frac{g_m(t)\,(r_b + r_e + Z_n(t))^2}{2\beta\,\mathrm{Re}(Z_n(t))} + \frac{(r_b + r_e + Z_n(t))^2}{2g_m(t)\,\mathrm{Re}(Z_n(t))\,\mathrm{Re}(Z_{be})^2} \tag{3-19}$$

g_m and Z_n are time-dependent variables because the modeling of the first stage of the mixer has been based on a small signal model of the transistor in the previous calculation. As the mixer is not a linear device, g_m and Z_n are not constant values. In [Xavier97], a model used to predict the noise figure of the HBT mixer is presented by splitting the influence of LO harmonics in the noise figure:

$$\begin{aligned} NF = {} & 1 + \frac{r_b + r_e}{\mathrm{Re}\,(Z_{-1})} + \frac{(r_b + r_e + Z_{-1})^2}{2\beta\,\mathrm{Re}(Z_{-1})}\,g_{-1} + \frac{1}{2g_1\,\mathrm{Re}(Z_{-1})} + \frac{(r_b + r_e + Z_{-1})^2}{2\,\mathrm{Re}(Z_{-1})\,r_\pi^2}\;\frac{1}{g_1} \\ & + \frac{Y_0}{Y_1\mathrm{Re}\,(Z_{-1})}\left((r_b + r_e + \mathrm{Re}(Z_0)) + \frac{(r_b + r_e + Z_0)^2}{2\beta}\,g_0 + \frac{1}{2g_0} + \frac{(r_b + r_e + Z_0)^2}{2R_\pi^2}\;\frac{1}{g_0}\right) \\ & + \frac{Y_{-1}}{Y_1\mathrm{Re}\,(Z_{-1})}\left((r_b + r_e + \mathrm{Re}(Z_1)) + \frac{(r_b + r_e + Z_1)^2}{2\beta}\,g_1 + \frac{1}{2g_{-1}} + \frac{(r_b + r_e + Z_1)^2}{2R_\pi^2}\;\frac{1}{g_{-1}}\right) \end{aligned} \tag{3-20}$$

where the rows of Eq. 3-20 are the noise contribution from RF, DC, and image frequencies to IF output, respectively. All three rows have a similar structure: thermal noise from resistances, base shot noise contribution, and collector shot noise contribution, which are the elements multiplied by $(1/g_i)$.

3.3.2.2.1 Influence of Mixer Design on the Noise Figure Two main parameters that influence the noise figure of the differential pair and that must be taken into account when designing a mixer can be distinguished when analysing Eq. 3-20.

The base and emitter resistances r_b and r_e are the only parameters of the transistors that affect thermal noise and that can be modified by the designer. To reduce the noise generated by r_b and r_e the number of base-emitter contacts and the emitter area must be as high and large as possible. However, the possible emitter area is limited due to parasitic capacitance c_π, which is proportional to the emitter area. This capacitance affects impedance Z in Eq. 3-20. Therefore, depending on the RF frequency, a balance must be struck between reducing thermal noise and reducing gain, which creates a rise in the noise figure due to the higher influence of noise from consequent stages.

The transconductance g_m is directly proportional to the collector current I_C, and this current is set when polarizing the mixer. If the transistor parameter β is high, the base shot noise contribution can be neglected and I_C should be increased. However, if β, which is frequency dependant (as seen in Eq. 3-21) is not high enough, then shot noise of I_b influences the noise figure and I_C should be reduced. The high-frequency small signal current gain [Gray84] is:

$$\beta(j\omega) = \frac{\beta_0}{1 + \beta_0 \dfrac{C_\pi + C_\mu}{g_m} j\omega} \tag{3-21}$$

where C_π is the base-emitter parasitic capacitance and C_μ is the base-collector parasitic capacitance, β_0 is the low frequency current gain and g_m the transconductance of the transistor.

Another consideration can be made from Eq. 3-20: The noise contribution of the second and third row can be minimised by filtering image and IF frequencies.

3.3.2.2.2 Influence of LO Power on the Noise Figure Once the mixer has been fabricated, there is a way to influence the noise figure, as can be seen in Eq. 3-20. The LO signal has great influence on the noise figure primarily because g_m is directly proportional to LO power. In addition, the LO signal has additional influence on mixer noise: If the switching of the four transistors in the mixer core had been ideal (see Figure 3-11), then only two transistors would have been constantly conducting and only two transistors would have been generating noise. However, there are small intervals when all four transistors are switched on simultaneously. The length of this interval depends on the LO signal, specifically its voltage level and shape.

3.3.2.3 Linearity in Gilbert Mixers Gilbert mixer linearity depends mainly on its first stage, which transforms the voltage input signal into a balanced current. This function is carried out by the differential input pair that makes up the amplification stage. Its behaviour can be defined

by a hyperbolic tangent function presented in Eq. 3-7 and included in Eq. 3-22.

$$V_{od} = 2I_C R_C \tanh\left(\frac{-V_{RF}}{2V_T}\right) \tag{3-22}$$

In section 3.3.2.1 in Eq. 3-10, a linear conversion has been considered by equating tanh(x) with x, assuming that the input signal is a small one. However, when analysing mixer linearity, this assumption cannot be made because high input signals are used to test the mixer.

To obtain varying output harmonics, the tanh(x) function is approximated by its Taylor series as shown in Eq. 3-23:

$$\tanh(x) = \alpha_1 x - \alpha_3 x^3 + \cdots \tag{3-23}$$

If the input signal of the mixer is a two-tone signal, then it can be expressed as shown in Eq. 3-24:

$$x(t) = A\cos\omega_1 t + A\cos\omega_2 t \tag{3-24}$$

where frequency ω_1 is close to frequency ω_2 and A is the signal amplitude. The output signal is obtained by substituting Eq. 3-23 in Eq. 3-22. This is shown in Eq. 3-25:

$$\begin{aligned}\tanh(x(t)) = &\left(\alpha_1 + \frac{9}{4}\alpha_3 A^2\right) A\cos\omega_1 t + \left(\alpha_1 + \frac{9}{4}\alpha_3 A^2\right) A\cos\omega_2 t \\ &+ \frac{3}{4}\alpha_3 A^3 \cos(2\omega_1 - \omega_2)t + \frac{3}{4}\alpha_3 A^3 \cos(2\omega_2 - \omega_1)t + \cdots\end{aligned} \tag{3-25}$$

Linearity is measured through the IP3 parameter, which is the theoretical point where output components at ω_1 and ω_2 have the same amplitudes as those at $2\omega_1$-ω_2 and $2\omega_2$-ω_1. If input amplitude A is small enough to guarantee that $\alpha_1 >> 9\alpha_3 A^2/4$ [Razavi97], then the IP3 point is given by Eq. 3-26:

$$|\alpha_1| A_{IP3} = \frac{3}{4}|\alpha_3| A_{IP3}^3 \tag{3-26}$$

where A_{IP3} is the normalized input signal amplitude at IP3 point as shown in Eq. 3-27 and output IP3 is given by $\alpha_1 A_{IP3}$:

$$A_{IP3} = \sqrt{\frac{4}{3}\left|\frac{\alpha_1}{\alpha_3}\right|} \tag{3-27}$$

In the input stage of a Gilbert cell, which is a differential pair, the α_1 and α_3 coefficients can be approximated by $\alpha_1 = 1$ and $\alpha_3 = 1/3$ for $-0.55 < x < 0.55$. As $x = V_{RF}/2V_T$, this means inputs up to ± 28.6mV for a bipolar differential pair operating at $T = 300$K. If the input signal amplitude is

the maximum signal, 28.6mV, which corresponds to –11.84dBm for a 50Ω input impedance, then the maximum input IP3 is as shown in Eq. 3-28:

$$\mathrm{IP3} = 20\log A_{IP3} + P_{IN} = 20\log\left(\sqrt{\frac{4}{3}\left|\frac{\alpha_1}{\alpha_3}\right|}\right) + P_{IN} = -5.82\,\mathrm{dBm} \tag{3-28}$$

As can be seen in previous equations, Gilbert cell linearity can be approximated by a mathematical function that is not dependent on the values of the elements that form the circuit (transistors, resistors, etc.). Theoretically, the HBT pair in the amplification stage has a linearity limit near –5dBm. This is the maximum IP3 value obtained in a Gilbert cell, but this value can fall if the layout of the circuit is not carefully designed or perfect switching is not achieved. To obtain the maximum IP3 value, a design must follow these recommendations:

- The switches in the mixer core should be made of small transistors, reducing base-emitter capacitance of switches and decreasing transition time. Linearity is improved because third-order intermodulation currents are generated only during transitions[Maas87].
- Layout techniques such as common centroid should be used to achieve equal branches in the Gilbert cell.
- The LO signal in the mixer core (see Figure 3-11) greatly influences linearity. It must drive enough power to quickly switch transistors within minimum transition time. However, an excess of power may charge the C_{be} parasitic capacitor of transistors in the mixer core, producing undesired current peaks[Lee98].

3.3.2.4 Local Oscillator Isolation Local oscillator isolation, which depends on differential structure, is increased by assuring symmetry between the two sides of the differential Gilbert cell.

3.3.2.5 Linearising Techniques The only way to increase linearity is by modifying the value of the parameters included in Eq. 3-22. There are two methods widely used to linearise Gilbert cells: the inclusion of emitter degeneration [Gray84] and the use of a class-AB input stage to replace the HBT differential pair from the amplification stage[Gilbert00].

Emitter degeneration consists of including emitter resistors in the transistor pair from the RF stage. This is a very popular way to extend the linear range of operation. The improvement factor in the differential pair is approximately equal to I_eRe, with I_e and Re representing the emitter current and the resistor value, respectively. However, the use of emitter degeneration to improve linearity involves some consequences in gain and noise:

- Voltage gain is reduced by approximately the same factor by which the input range is increased.

- A new contributor is added to the voltage noise defined by Eq. 3-29:

$$v_{nRe}^2 = 4kTRe \tag{3-29}$$

which is the thermal noise resulting from emitter degeneration. In addition, because of voltage gain reduction in the differential input stage, the contributions to noise from following stages become more significant.

There are two kinds of degeneration that can be included in the emitter: resistive or inductive. Resistive degeneration is used when the RF signal is a low frequency or a wideband signal and shows a lower gain than the latter. Inductive degeneration is used with high frequency and narrowband signals.

The bisymmetric class-AB topology based on translinear principles is a linearising technique that has no inherent gain compression [Gilbert00]. The input stage diagram is shown in Figure 3-14.

In this input stage, the relationship between I_{RF} and the difference between I_1 and I_3 is shown in Eq. 3-30:

$$I_{RF} = (I_1 - I_3) \tag{3-30}$$

resulting in a linear operation, provided that the input signal is a current.

This stage has several points that must be taken into account when designing a mixer:

- The input resistance of this stage is:

$$R_{IN} = \frac{V_T}{2I_1} \tag{3-31}$$

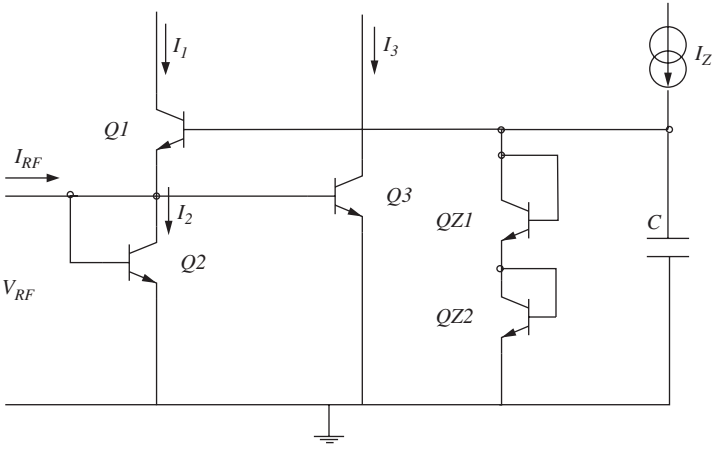


Figure 3-14 Simplified class-AB input stage

From Eq. 3-31, it can be seen that a very low value of I_1 should be used to obtain a 50Ω input resistance. However, this current value would result in poor gain and consequently higher noise.

- The mixer gain associated with this input stage is:

$$G_V = R_C g_{mRF} \frac{4}{\pi} \tag{3-32}$$

When comparing Eq. 3-32 with the gain of the differential pair in Eq. 3-10, it can be seen that the gain in mixers employing class-AB as the input stage is twice that obtained in mixers with a differential pair in the input stage. However, in class-AB, the collector current I_c is lower in order to facilitate 50Ω matching, resulting in lower g_{mRF}.

- The noise figure equation for mixers that use class-AB as the input stage is quite similar to the noise figure in mixers with Gilbert cells. Nonetheless, it includes some differences:
- There are three transistors in the input stage, so there are three additional noisy current sources associated with shot noise from I_c and I_b.
- The voltage gain is not high enough and the noise from the mixer core and the buffer influences the mixer's global noise figure.

When AB topology does not completely meet linearity requirements, it is sometimes possible to combine both methods and to include emitter degeneration in all three transistors of the class-AB stage.

3.3.3 Combined RF Pre-Amplifier and Mixer Design

As previously explained, a relatively high-gain receiver configuration has been chosen. For this reason, the RF mixer has been implemented using a differential input amplifier plus a Gilbert cell. Figure 3-15 shows the final simplified circuit diagram.

Taking previous design considerations into account, the input impedance of the Gilbert cell has been set to optimise the power consumption, gain, NF, and linearity of the entire RF mixer. If the input impedance is increased by degenerating the Gilbert cell, the gain of the cell will be lower and the NF will be higher. Those effects can be minimised by increasing the gain of the preceding RF amplifier. As the load of the amplifier will be higher due to higher input impedance of the Gilbert cell, no extra power will be needed to increase the gain of the RF amplifier. This results in low power consumption and the improvement of linearity of the entire RF mixer as well as the linearity of the Gilbert cell.

On the other hand, to avoid degrading the performance of the RF mixer, the LO power level must guarantee the appropriate switching performance of the mixer core. The local oscillator power level should be between –10dBm and –3dBm in the designed Gilbert cell, which input impedance

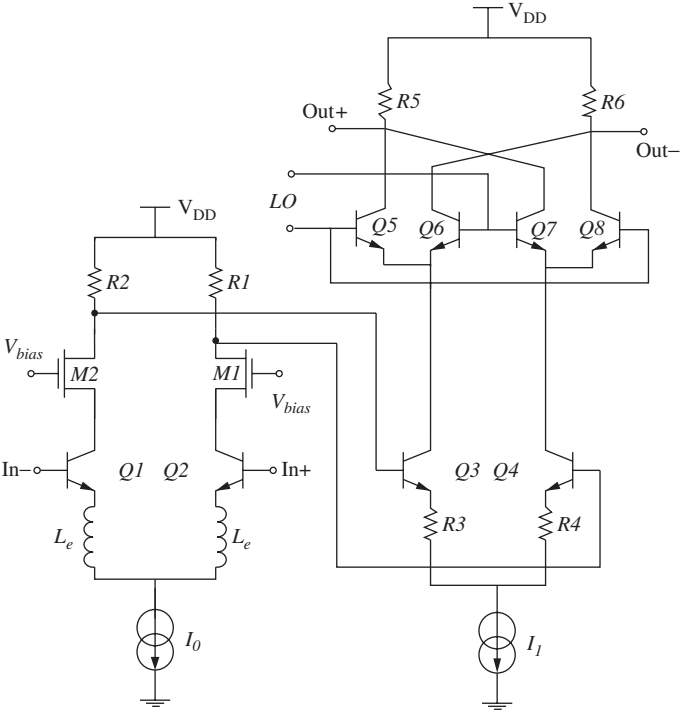


Figure 3-15 Simplified schematic of the down-conversion stage (differential amplifier + Gilbert cell)

differs from the standard 50Ω. Due to this high power value, the isolation between the LO input and the IF output must be high enough to avoid feedthrough and interference problems. To suppress the LO signal at the IF output, a differential Gilbert cell and external filtering have been used.

3.3.4 Layout Considerations and Simulation Results

Figure 3-16 shows a microphotograph of the designed frequency down-conversion block. The pre-amplifier and its emitter degenerating inductances can be identified in the middle of the microphotograph, just above the down-conversion mixer. The RF, IF, V_{DD}, and GND pads surround both blocks (pre-amplifier and mixer).

Common centroid techniques have been used with all the elements of the pre-amplifier and the mixer to avoid linearity degradation and to improve LO/RF and LO/IF isolation. That plays a big part in avoiding re-radiation of the LO signal through the LNA and the antenna as well as LO signal saturation or interference with the IF signal. RF pads have a hexagonal shape and are manufactured with only the top thick metal layer to minimise parasitic capacitance. The size of the pre-amplifier and mixer chip (including decoupling capacitors and pads) is $1.25 \times 1.1 mm^2$.

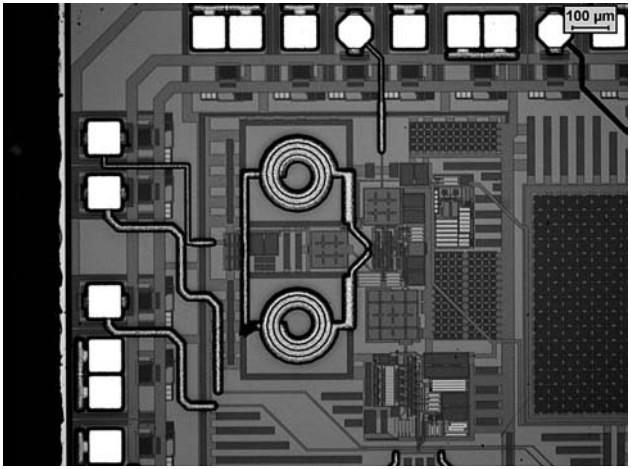


Figure 3-16 RF pre-amplifier and mixer microphotograph

Double pads are used for V_{DD} and GND to allow double bondwires in order to reduce their parasitic inductance. This minimises AC ground and supply loops resulting from bondwire and package parasitic inductances, reducing the risk of pre-amplifier oscillation.

As in the case of the LNA, different parasitic effects have been taken into account in order to perform simulations of realistic situations. Effects of PAD parasitic capacitances, bondwire inductances, bondwire coupling between different pins, and package parasitics are included in the simulation setup to facilitate the obtaining of realistic results.

The specification values reported in the previous chapter and post-layout results of the down-conversion block are shown in Table 3-5.

The design presents a lower NF and current consumption than specified, but at the cost of lower gain. The extra needed gain, caused by the low gain of the mixer, will be supplied by the IF amplifier. This will ensure that the initial overall receiver gain specification will be met. The linearity, OIP3, is just 1dB (0.5dBm) lower than specified (1.5dBm). It will only slightly influence the interference blocking capacity of the receiver, resulting in satisfactory front-end performance.

TABLE 3-5 Post-layout results

Parameter	Specifications	Post-layout	Unit
S11	< –10	–20.2	dB
OIP3	1.5	0.5	dBm
Gain	23	18.1	dB
NF	6.2	5.6	dB
Current	<13	5.9	mA

3.4 IF Limiting Amplifiers and Filters

The design of two IF LC filters is covered in the IF stage. The first one is located next to the RF down-conversion mixer. The second one is located between the first and second IF limiting amplifiers (see Figure 3-1). The IF filters provide the following functions:

- They define and shape the noise bandwidth to be amplitude-quantized by the 1bit ADC.
- They provide the required selectivity to protect the IF limiting input from spurious signals that pass through the RF SAW filters, typically 20MHz wide.
- They attenuate undesired second mixer output products, such as the LO leakage or mixer second harmonics, to levels that will not block the IF limiter amplifier.
- They can reject spurious common mode and/or differential signals generated by high-level on-chip sources, such as reference clock harmonics.

Two IF limiting amplifiers have been considered in the system analysis. Both are preceded by an LC filter, which is located next to the mixer and the first amplifier respectively. They provide the gain required to digitalise the incoming GPS signal. The noise figure is not a key parameter because of its low contribution to the total noise, as stated by the *Friis* equation [Razavi97], since it is not included in the early stages of the front-end, but after the LNA, the RF amplifier, and the down-conversion mixer.

Figure 3-17 shows the basic cell of the IF amplifier. It is a differential common source architecture due to its high voltage gain as well as its

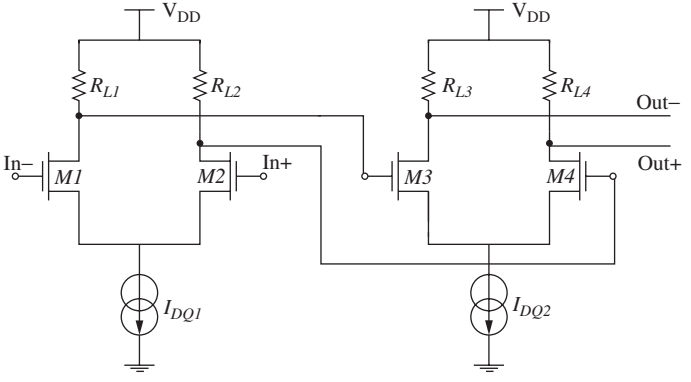


Figure 3-17 IF basic cell amplifier schematic

high input and output impedance. The load for the first amplifier (IF1) comes from the second IF amplifier (IF2) and the second IF filter, where the load for the second IF amplifier (IF2) comes from the 1bit ADC.

As mentioned before, implementing a 1bit ADC is considered to be the last stage in the chain of the front-end. Therefore, above a minimum level, amplitude of the ADC input signal is insignificant because only negative-to-positive transitions, or vice versa, are detected. For this reason, clamping diodes can be used without any information loss, as shown in Figure 3-18. In addition, the amplitude of the amplifier output signal will be limited. Clamping of the output signal will allow the input switches of the ADC latches to work properly, minimising any current leakage. It is important to keep in mind that the clamping diodes also load the amplifier. Therefore, small diodes are recommended to avoid degrading of the frequency response.

To implement the amplifier chain, various basic stages are connected in cascade to obtain the required gain. Thus, IF1 is built with three basic stages in cascade and an output common drain stage to match the output impedance to the LC filter, as shown in Figure 3-19. The load resistance of the third basic stage has been decreased to 6kΩ in order to reach the required bias voltage for the common collector output stage. Figure 3-20 shows the IF2 amplifier, which consists of two basic stages.

Figure 3-17 shows the basic cell used for the IF amplifier. The load resistance (R_L), the bias current of the differential amplifier (I_{DQ}), and the width of the transistors (W) are considered to be design variables. The length of the transistors (L) is fixed at 1.3μm. Due to size mismatch problems, a larger value than the minimum 0.35μm is set to minimise the input offset of the differential pair.

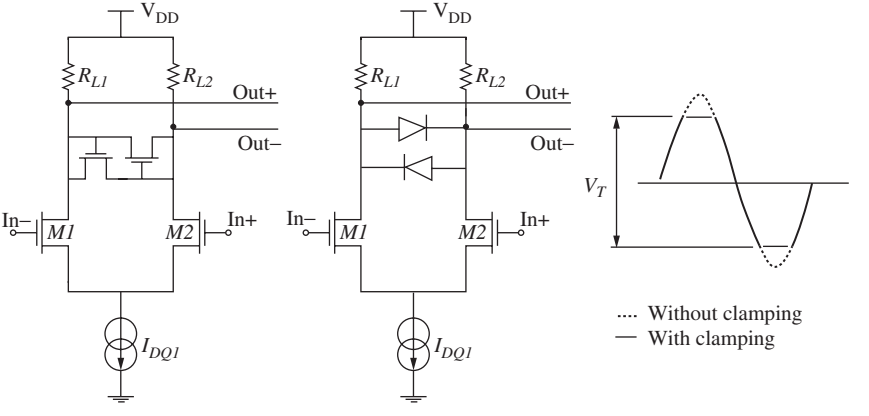


Figure 3-18 IF limiting amplifier with clamping diodes (diodes or MOS transistors)

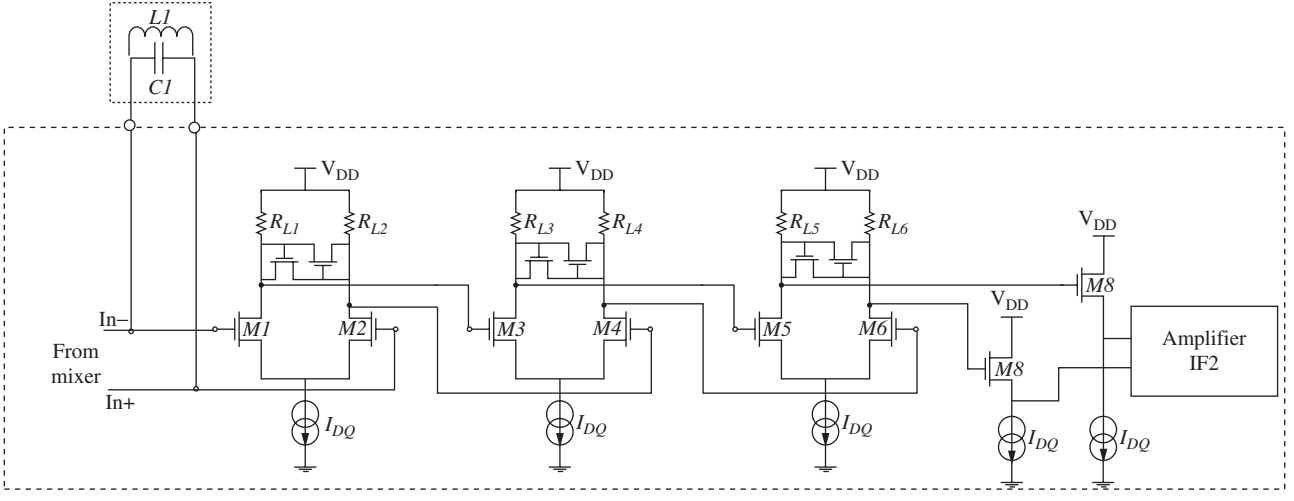


Figure 3-19 IF1 amplifier chain

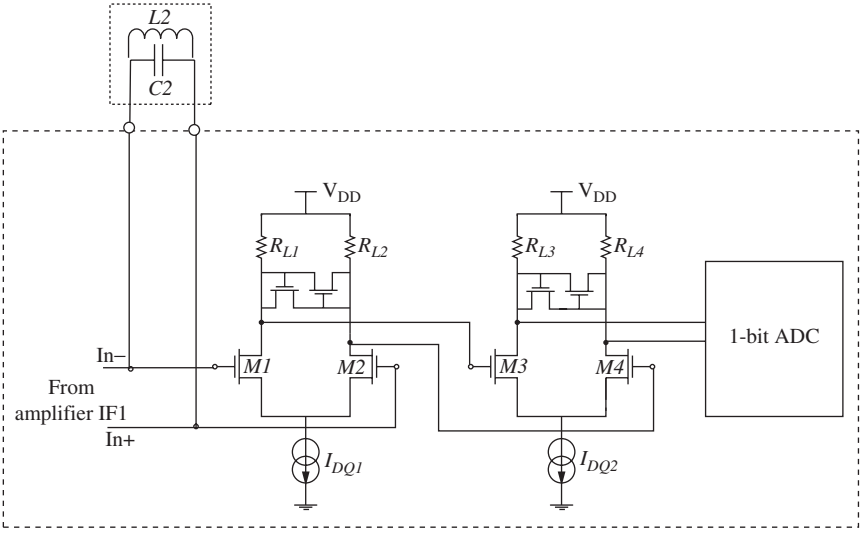


Figure 3-20 IF2 amplifier chain

By examining the IF amplifier small-signal equivalent circuit presented in Figure 3-21, the gain and the dominant pole of the system can be obtained from Eq. 3-33 and Eq. 3-34, respectively.

$$A_V = \frac{V_{out}}{V_{in}} \approx -g_{m1}.R_L \tag{3-33}$$

$$\omega_1 \approx -\frac{1}{C_1.R_1} \tag{3-34}$$

where Eq. 3-35 and 3-36 are as follows:

$$R_1 = \frac{r_0.R_L}{r_0 + R_L} \approx R_L \tag{3-35}$$

$$C_1 = C_{GD} + C_{BD} + C_L \tag{3-36}$$

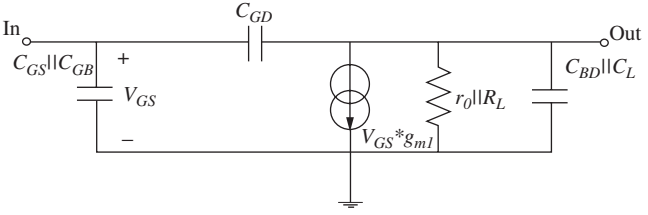


Figure 3-21 Simplified IF amplifier small-signal equivalent circuit

Therefore, the system transfer function can be roughly expressed as shown in Eq. 3-37:

$$A_V \approx -g_{m1}.R_L.\frac{\omega_1}{1+\omega_1} \tag{3-37}$$

where ω_1 is the frequency of the pole. Based on these equations and verified by simulations, optimal design variables values have been set to the values shown in Table 3-6.

The LC values of the external IF filters are shown in Table 3-7. The required extra capacitance to set the central frequency of the IF filter to 20.4MHz is added on chip.

3.4.1 Layout Considerations and Simulation Results

Figure 3-22 shows the layout of the IF amplifier. Common centroid techniques and dummy structures have been employed to minimise any

TABLE 3-6 Size of the transistors and load resistor values for the first stage of the IF amplifier

Transistor	W/L [μm]	Transistor	W/L [μm]	Resistor	R_L [Ω]
M_1-M_2	28/1.3	M_5 (I_{DQ})	60/3	R_{L1}-R_{L2}	11000

TABLE 3-7 Values of IF filter components

L1	2.7μH	*L2*	4.7μH
C1	43pF	*C2*	24pF

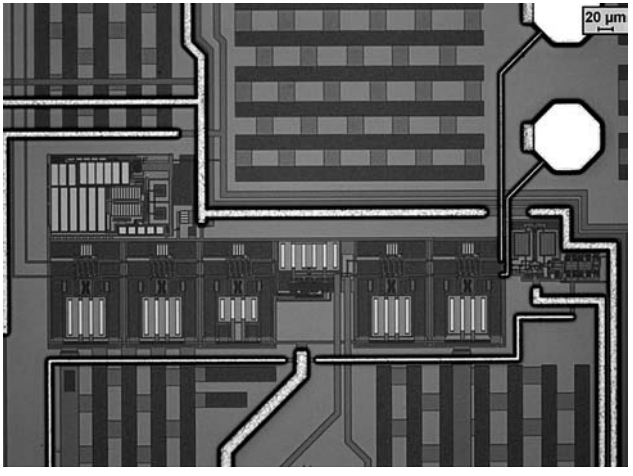


Figure 3-22 IF amplifier microphotograph

imbalance in the differential path. Several ground contacts have also been placed between the different stages of the IF amplifier to minimise any coupling through the substrate that could cause the amplifier to oscillate. That is important as stages are placed close to each other and the gain is high (85dB). Finally, two internal pads have been placed at the output of the second IF limiting amplifier for test purposes. The size of the IF amplifier is approximately 630x270μm^2.

Figure 3-23 shows the IF amplifier gain. It can be observed that it meets the gain specification set in the previous chapter. Moreover, the band-pass shape centred in ~20.4MHz can be also observed. The -3dB passband bandwidth is 5.2MHz. Table 3-8 shows mean post-layout results and the specification values of the IF amplifier and filters. The amplifier gain has been oversized to enable the detection of the navigation signal in difficult environments such as a street surrounded by very high buildings. The passband bandwidth is smaller than the specified 6MHz. This fact will cause the C/N_0 to degrade due to precorrelation filtering of only 0.2dB, which is not high but assumable.

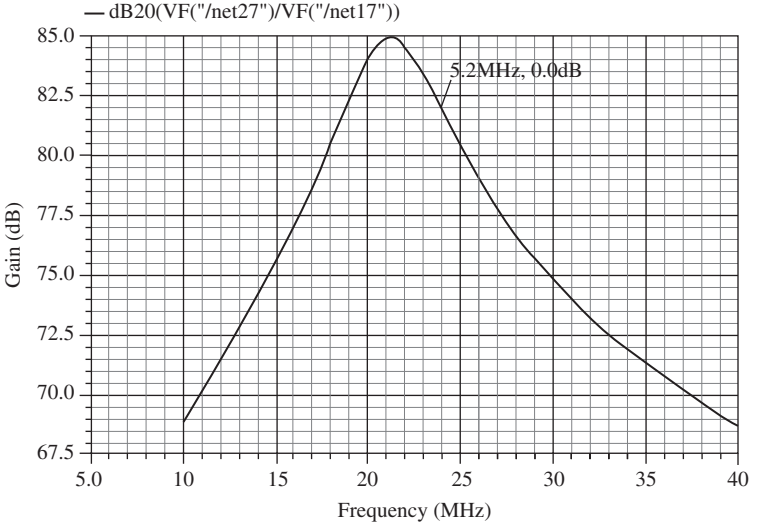


Figure 3-23 IF limiter amplifier post-layout simulation gain results

TABLE 3-8 IF amplifier and filter performance

	Spec.	Post-layout	Unit
G	>42	85	dB
BW	6	5.2	MHz
Current	3	2.4	mA

3.5 Analogue-to-Digital Conversion (ADC)

As mentioned in the previous chapter, the 20.42MHz down-converted signal is subsampled at a sampling rate of 16.368MHz, down-converting the incoming signal to a second IF of 4.092MHz.

The employed sampling rate, quantisation, and precorrelation bandwidth are all related and have a combined effect on the implementation losses in the receiver. These effects differ, depending on whether the signal is corrupted by Gaussian noise, other types of interference, or both. As mentioned in the previous chapter, in the presence of Gaussian noise, the degradation caused by quantisation depends on the precorrelation bandwidth and the number of bits. For an optimum ratio of maximum threshold to RMS noise level, the number of bits should be as high as possible and the degradation caused by quantisation as low as possible. For a precorrelation bandwidth of five times the chipping rate (1.023MHz) and an analogue-to-digital converter of ≥3bits, the typical degradation is below 0.5dB.

However, as mentioned in the previous chapter, a 1bit quantisation has been selected even when higher-degradation was introduced. This allows for the design of a simpler, lower-power receiver without the need for automatic gain control. As the IF frequency is relative low with a period of approximately 50ns, the complementary metal oxide semiconductor (CMOS) A/D aperture time poses no problem. The 1bit A/D converter has been implemented using a latch, as can be seen in Figure 3-24.

The operation of the latch can be divided into two stages: comparison and data storage. During data storage or the noncomparison stage (clock 3.3V), *M6* and *M7* transistors behave like short circuits, allowing the input signal to be stored in the *C1* and *C2* capacitors. In addition, the positive feedback loop is disabled by means of *M5*. For the comparison stage (clock 0V), *M5*, *M6*, and *M7* transistors are open circuit, resulting in isolated input and an activated positive feedback loop. The differential

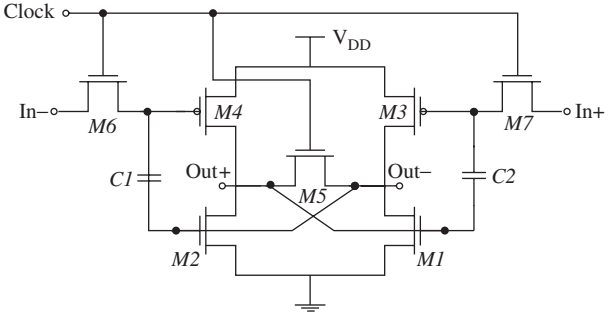


Figure 3-24 Latch comparator

voltage stored in the previous stage biases *M3* and *M4* transistors. *M3* and *M4* will drive current in an uneven way, dictated by the charge stored in *C1* and *C2*. This will unbalance the nodes Out+ and Out–. The positive feedback loop will set the outputs to V_{DD} or GND, depending on the case. Figure 3-25 shows voltage stored in the capacitors and the amplifier output signals.

3.5.1 Layout Considerations and Simulation Results

The main component of the ADC is the latch, as shown in the previous section. Figure 3-24 shows the circuit diagram for the latch composed of two 765fF capacitors and seven transistors, the sizes of which are shown in Table 3-9. The layout of the ADC is shown in Figure 3-26.

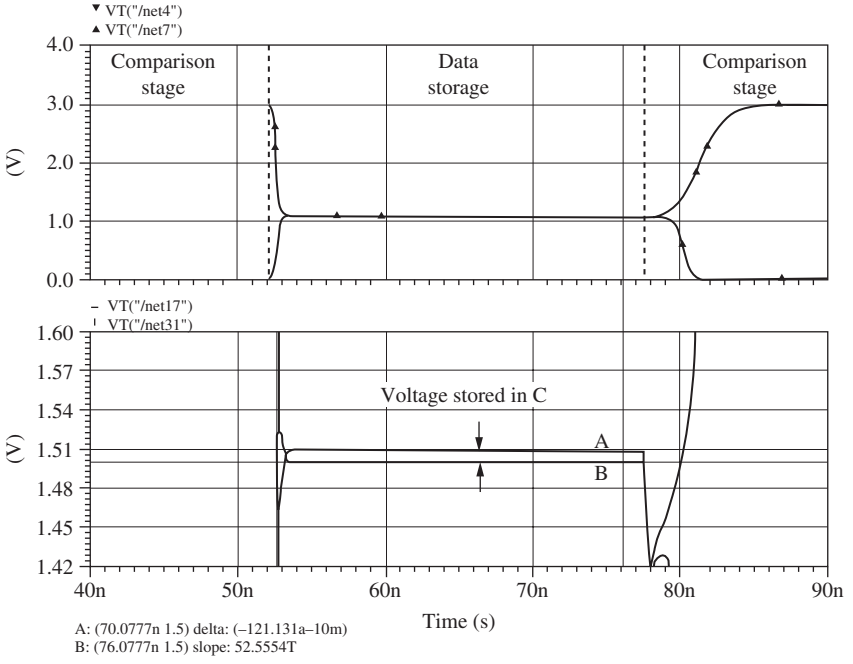


Figure 3-25 Time response of the latch

TABLE 3-9 Size of latch amplifier transistors

Transistors	Width (W)	Length (L)	Unit
M1–M4	8	1	µm
M5	3	0.35	µm
M6–M7	2	0.35	µm

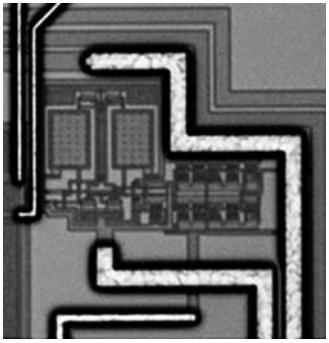


Figure 3-26 Layout of the ADC

TABLE 3-10 Consumption, operation frequency, and offset of the ADC

Consumption	Operation Frequency	Offset voltage
1.5mW	16.368MHz	± 12.5mV

Table 3-10 shows the current consumption, the operating frequency, and the ADC input offset voltage. While the first two have been obtained from simple post-layout simulations, the offset has been obtained through a *Montecarlo* analysis of 200 samples (Figure 3-27).

To see the importance of metastability errors, time response simulations of different input signals have been carried out. The results show that no metastability problems arise with the working frequency (~20MHz).

Due to the nature of the latch amplifier, the signal at the output is correct only 50 percent of the time. To provide a constant valid output signal, a flip-flop is placed at the output of the latch. The flip-flop provides a single output synchronised with a clock from the two outputs of the latch amplifier. Figure 3-28 shows the circuit diagram for the flip-flop, which consists of logical gates.

3.6 Frequency Synthesiser

The frequency synthesiser has been implemented by means of a PLL. The simplified block diagram of which is shown in Figure 3-29.

The feedback loop causes both input signals of the phase frequency detector (PFD), the output of the pierce oscillator, and the output of the pulse swallow divider to lock, thereby creating a voltage controlled oscillator (VCO) output frequency (f_{out}) multiple of the reference frequency (f_{Xtal}). The feedback loop takes part of the output signal and divides its frequency to compare the resulting signal with a reference signal. The difference between these two signals is converted into a voltage that

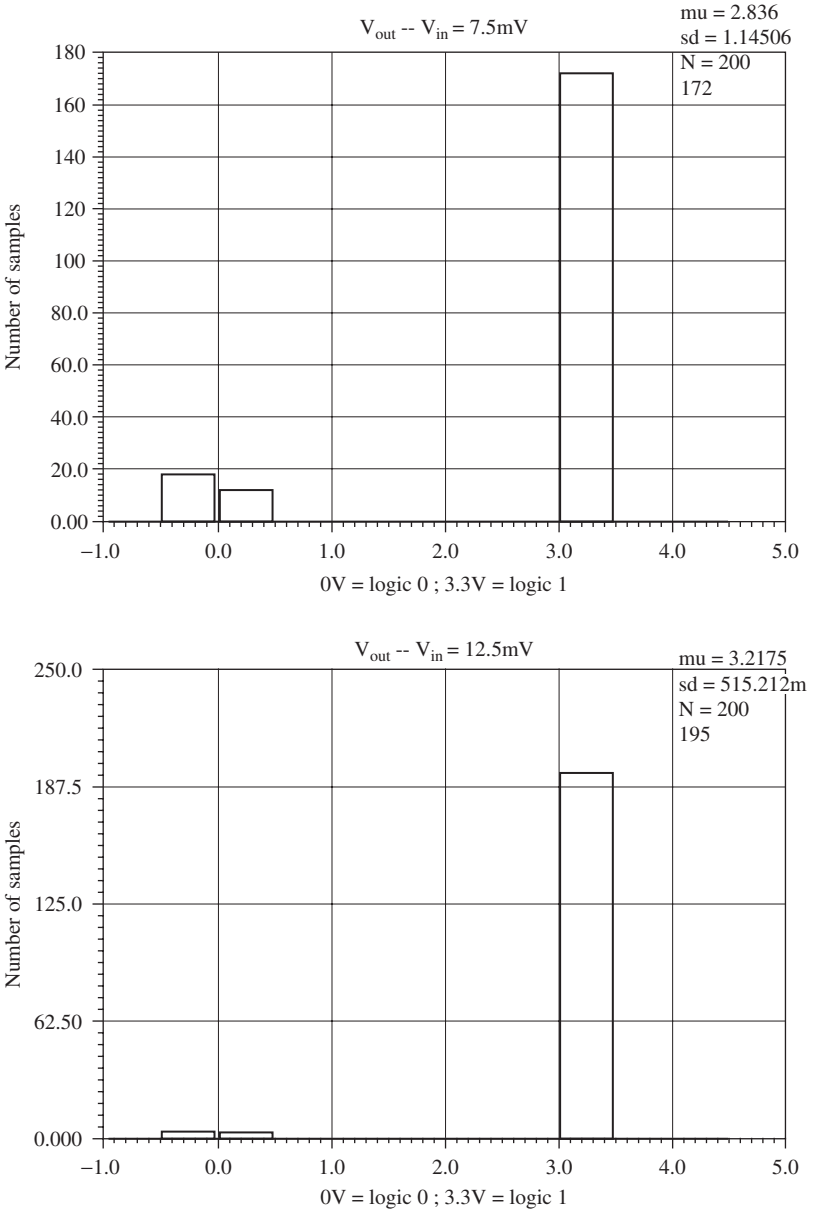


Figure 3-27 Montecarlo analysis simulation results for input voltage of ±7.5mV (top) and ±12.5mV (bottom) out of 200 samples

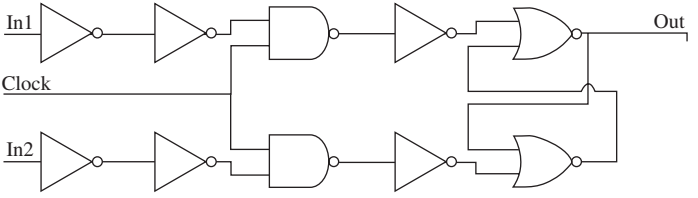


Figure 3-28 Flip-flop block diagram

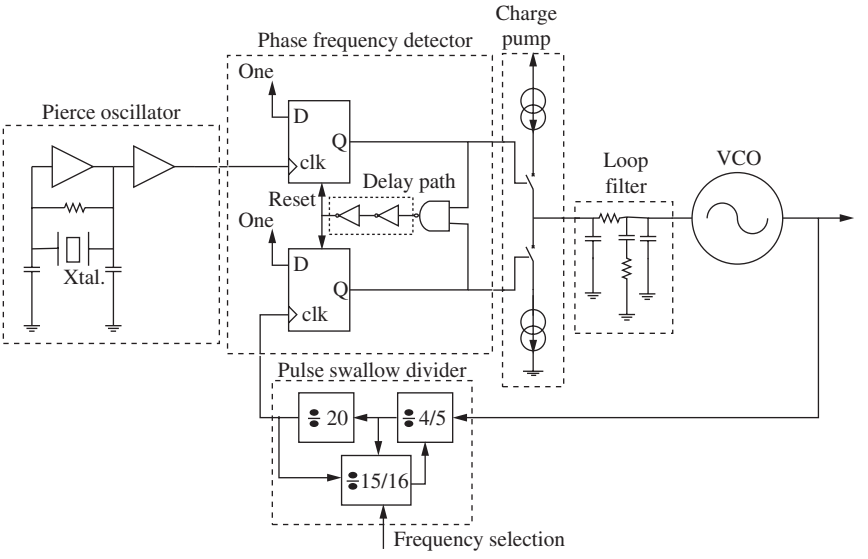


Figure 3-29 Simplified block diagram of the implemented PLL

controls the frequency of the output signal. When the divided signal is equal to the reference signal, the output is phase locked.

The value of the synthesised frequency at the VCO output is determined by the division factor of the frequency divider compared to the output frequency of the pierce oscillator. In the design example, the PLL must provide one of two frequencies, depending on the operation mode: 1554.69MHz or 1571.328MHz, which are set by the frequency selection pin of the pulse swallow divider.

These frequencies, as shown in Figure 3-29, are obtained by means of a pulse swallow divider, which divides the VCO output frequency by 95 in the first case and by 96 in the second case. After that, the PFD compares the resulting signal with the reference frequency of 16.638MHz, which is generated by the pierce oscillator. The output of the PFD then controls the charge pump to set the VCO tuning voltage.

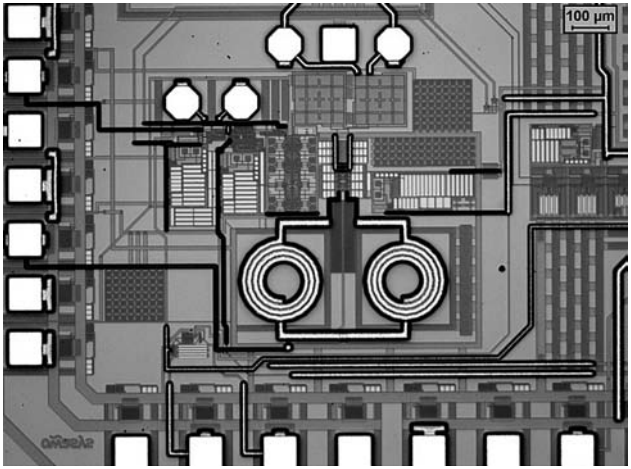


Figure 3-30 Frequency synthesiser layout

The layout of the complete PLL is shown in Figure 3-30 and it occupies an area of 870×615µm^2. Table 3-11 shows the required specifications and the post-layout simulation results for the PLL. The quartz crystal and loop filter are external to the integrated circuit (IC).

It can be seen that most of the requirements are fulfilled by the design example. The output power is between the specified 0dBm and 3dBm for a 50Ω load, being the output power for the mixer load lower due to its impedance. The required frequency range is also covered by the PLL. Although the requirement of the K_{VCO} is lower than specified, the PLL generates the required signal frequencies and therefore meets the standards of the application.

The power of the second harmonic is higher than specified when the control voltage is equal to 0.5V, which is also acceptable because of the narrowband characteristic of the front-end. Phase noise at the working frequency fulfils the specification of -90dBc/Hz, however with GPS and Galileo being spread spectrum systems, phase noise is not a critical

TABLE 3-11 Post-layout simulation results for the PLL

	Specified		Post-layout		
Parameter	**[2.8V]**	**[0.5V]**	**[2.8V]**	**[0.5V]**	**Unit**
Output power	0~3	0~3	1.09	1.26	dBm
Frequency	1.544	1.571	1.49	1.71	GHz
Phase noise @100kHz	–90	–90	–83	–97	dBc/Hz
2. order harmonic	–23	–23	–22.5	–13.2	dBc
Current consumption	<9	<9	10	10	mA

issue and even a value around –83dBc/Hz at 100kHz offset is acceptable [SONY CXA1951AQ] [uNAV un8021C] [Freescale MRFIC1505] [ST STB5610] [zarlink GP2015] [Atmel ATR0603]. Finally, the resulting consumption is around 10 percent higher than specified, which was required to reach this level of performance. This will solely affect the low power consumption feature of the front-end.

The following subsections describe the different parts of the implemented PLL in detail: the voltage controlled oscillator, pulse swallow divider, phase frequency detector and charge pump, pierce oscillator, and loop filter.

3.6.1 Voltage Controlled Oscillator (VCO)

The VCO is the component that generates the LO input signal for the mixer at a given frequency. To have an accurate signal frequency, the VCO is controlled by a PLL, which corrects the frequency and phase differences and ensures frequency stability. Figure 3-31 shows the circuit scheme of the completely integrated differential VCO of the design example. An LC tank has been selected because of its integration abilities in comparison with other alternatives. Two cross-coupled transistors, *M1* and *M2*, generate the negative impedance required to cancel the losses associated with the non-ideal LC tank. There are two advantages of this architecture: Use of PNP transistors is avoided and a higher control voltage tuning can be employed.

The main parameters of the output signal are frequency, amplitude, and phase noise. The VCO of the design example is built by means of a resonating LC tank. Therefore, the frequency is set by the control voltage that varied the capacitance of a resonating LC tank. The power

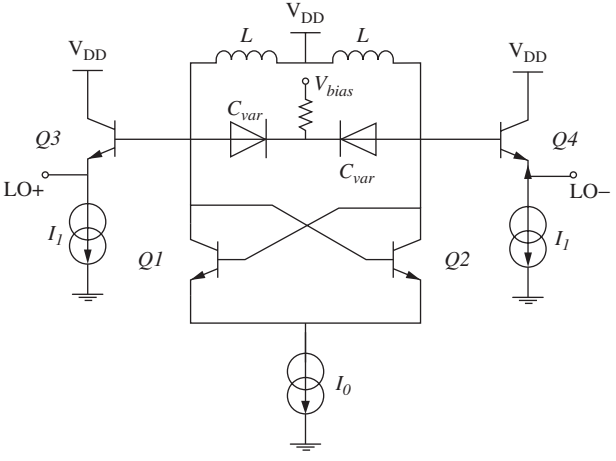


Figure 3-31 Simplified scheme of the VCO

can be determined by VCO's coupled transistor stage gain, and impedance matching between the VCO output and the mixer input. The oscillator phase noise depends on the quality factor of the LC tank; the noise figure of the amplifier, which creates a negative resistance; and the energy in the LC tank.

The simplest way to reduce phase noise is by increasing the resonator energy through the application of higher voltage to the tank. In the current design, an emitter-coupled pair with cross feedback is used as a negative resistance, which is responsible for the undamping of the resonator. The limit of the maximum oscillation amplitude will depend on the feedback. The easiest way to implement the aforementioned feedback is by a direct coupling: No biasing network is required and very low power consumption can be achieved (see Figure 3-31).

The LC tank sets the frequency range where the VCO will oscillate. For the LC tank, an inductor (L) and a varactor (C) are required. The main parameters of the inductor are the inductance, the self-resonance frequency, and the quality factor, whereas those of the varactor are its capacitance, quality, and tuning range.

The performance of the inductor has been estimated by the spiral inductors and transformers simulator ASITIC [ASITIC], taking into account technological features such as parasitic capacitance of metal tracks and ohmic lines. A 2.5nH inductor has been designed with the fourth metal layer (low resistivity, thick metal) to reduce the ohmic lines associated and to enhance the quality factor (Q). A microphotograph of the inductor is shown in Figure 3-32.

The characteristics of the fabrication process allow the implementation of the varactor with a PN junction composed of P+ diffusion in an N-type well[Gutierrez07]. The capacitance, tuning range, and quality factor are defined by the technology, the configuration, and the size of the varactor. An interdigit varactor of 75 fingers with a length of 30μm and the minimum possible width and separation allowed by the technology has been designed for the LC tank of the VCO. The capacitance is

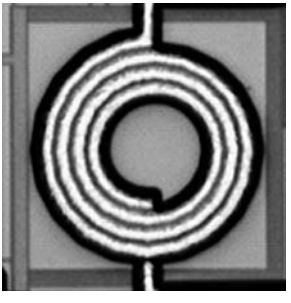


Figure 3-32 Microphotograph of the VCO inductor

2.5pF for a 0.5V control voltage and 1.5pF for 2.8V, resulting in a tuning range of 26.5 percent (simulation results).

Considering the inductance and capacitance previously obtained, a K_{VCO} of 254kHz/V could be obtained for the defined tuning range. However, this value is reduced due to the parasitic capacitances of the metal lines, transistors, and so on.

The VCO consists of three main parts: the LC tank, the negative resistance loop (see Figure 3-31), and an emitter follower stage. The latter works as a buffer, driving the load of the VCO, which is the mixer and pulse swallow divider.

As previously mentioned, the negative resistance loop compensates the losses of the LC tank to maintain stable oscillation; it consists of two cross-coupled transistors, as shown in Figure 3-31. Therefore, it could be thought that the value of the transconductance should be the same as the resistive part of the LC tank. However, this would not ensure oscillation. Therefore, a security factor between 2 and 3 has to be considered, as stated in[Craninckx-Steyaert98]. The selection of this security factor is a trade-off between the current consumption of the VCO and the risk of VCO oscillation failure due to process variation. In the design example, a security factor of 2 has been applied.

The post-layout results shown in Table 3-12 have been obtained by means of simulations.

The results meet most of the requirements. As explained for the PLL, the power of the second harmonic is higher than specified for the case of the control voltage being equal to 0.5V. This is acceptable because of the narrowband characteristic of the front-end. With Galileo and GPS being spread spectrum systems, phase noise is not a critical issue. Even a value around –83dBc/Hz at 100kHz offset is acceptable [SONY CXA1951AQ] [uNAV un8021C] [Freescale MRFIC1505] [ST STB5610] [zarlink GP2015] [Atmel ATR0603]. Phase noise postlayout simulation results showed that this requirement is fulfilled at the working frequencies of the PLL, although at the highest frequencies of the VCO's frequency is lower than specified, this is acceptable for a spread spectrum

TABLE 3-12 VCO post-layout simulation results

Corner	Vctr [V]	Pout [dBm]	Fout [GHz]	Freq. Tuning [%]	2.harm. Power [dB]	2.harm. Fout [GHz]	Phase Noise @ 100k [dBc/Hz]	Current [mA]
Spec.	0.5 2.8	0-3	1.717 1.408	±10	–23	—	–90	<6
Sim.	0.5	1.26	1.71	±6.96	–13.25	3.43	–81.2	6.3
	2.8	1.09	1.49		–22.55	2.98	–96.9	

system as explained previously. Finally, the frequency tuning is slightly lower than specified, but required working frequencies of 1554.69MHz and 1571.328MHz are within the required frequency range.

3.6.2 Pulse Swallow Divider

To compare the VCO output signal frequency with the reference *Xtal* frequency, a divider is required. For the design example, it consists of a dual modulus prescaler ($N = 4$, $(N+1)/N$), a program counter ($P = 20$), and a swallow counter ($S = 15/16$) (see Figure 3-33). Therefore, from Eq. 3-38 [Razavi97], a division ratio of 95 and 96 is obtained.

$$f_{out} = f_{in} / (NP + S) \tag{3-38}$$

where f_{in} is the output frequency of the VCO and f_{out} the signal frequency of the divider output that will be compared using a PFD with the *Xtal* signal. N is the division ratio of the prescaler, P is the division ratio of the program counter, and S is the division ratio of the swallow counter.

Figure 3-33 shows the architecture of the pulse swallow divider. Due to the high frequency of the incoming signal (1.575GHz), a prescaler has been implemented using emitter-coupled logic (ECL). The program counter and the swallow counter work at frequencies between 310MHz and 393MHz. Thus, CMOS logic has been used to minimise power consumption. Moreover, a comparator is required as an interface to convert the signal level from ECL to CMOS logic.

To work properly, signal delay through the different gates must be smaller than the duration of the incoming signal. Otherwise, pulses might be lost and a different division ratio will be obtained. Therefore, gates have been carefully designed to minimise delays, particularly in the swallow counter, which sets the prescaler divider ratio. The output frequency (16.368MHz) is compared to the reference frequency by the phase frequency detector.

3.6.2.1 Prescaler The high-frequency prescaler consists of three D flip-flops and two NAND gates (see Figure 3-34). The division ratio is controlled by a counter through the control modulus input (S) coming from the swallow counter. If the modulus control is "high," the division ratio will be 5. On the other hand, if the modulus control is "low," the division ratio will be 4.

Although requiring higher current, ECL logic has been chosen due to its high operation speed, which allows it to perform correctly at the desired frequencies of 1554.96MHz and 1571.328MHz. Required D flip-flops and NAND gates have been designed at transistor level with a differential architecture to load the output of the VCO differentially.

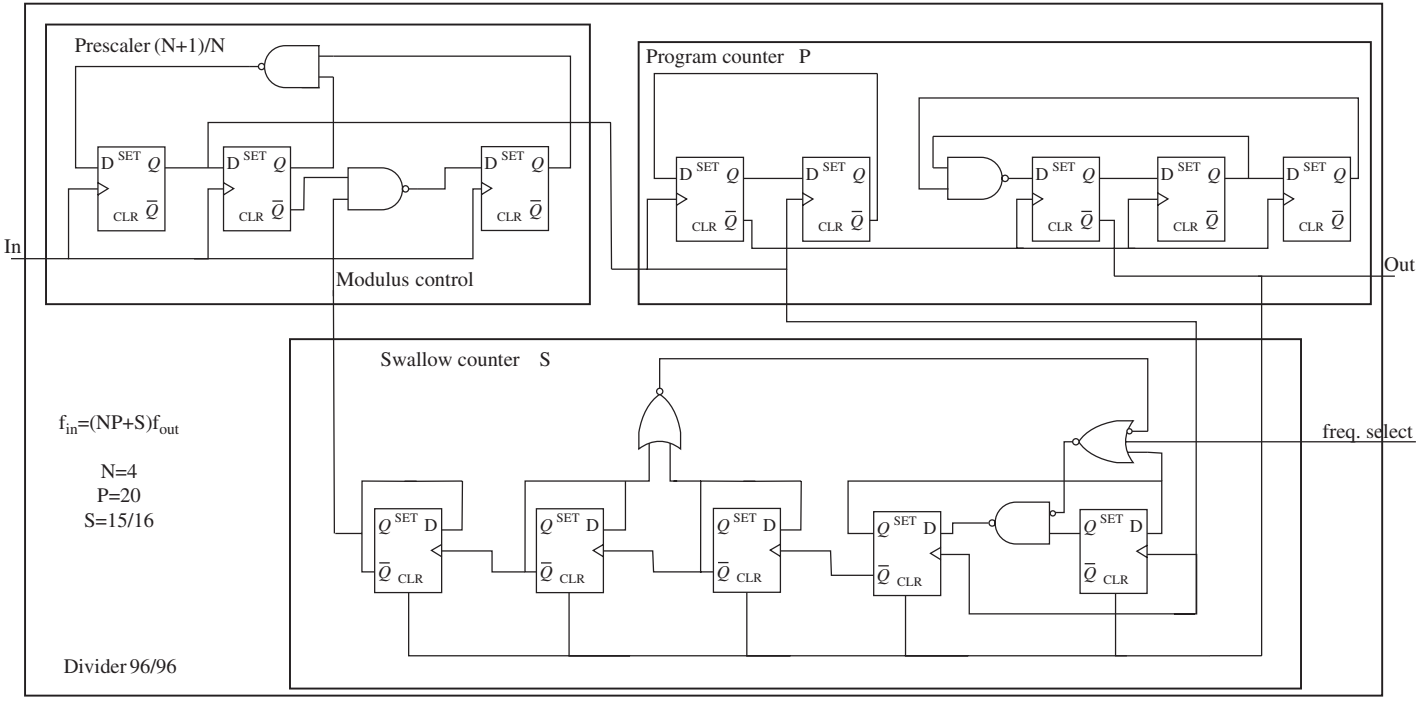


Figure 3-33 Pulse swallow divider block diagram

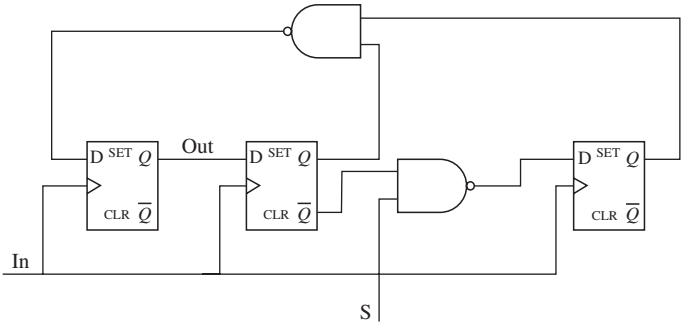


Figure 3-34 Diagram of the prescaler

These standard ECL architectures are shown in Figure 3-35 and Figure 3-36. The implemented D flip-flop consists of two differential master-slave latches. The operation of the flip-flop has two steps: In the first clock pulse, input data is stored; in the second clock pulse, the stored data is set as the output. Figure 3-37 shows the microphotograph of the layout of the prescaler.

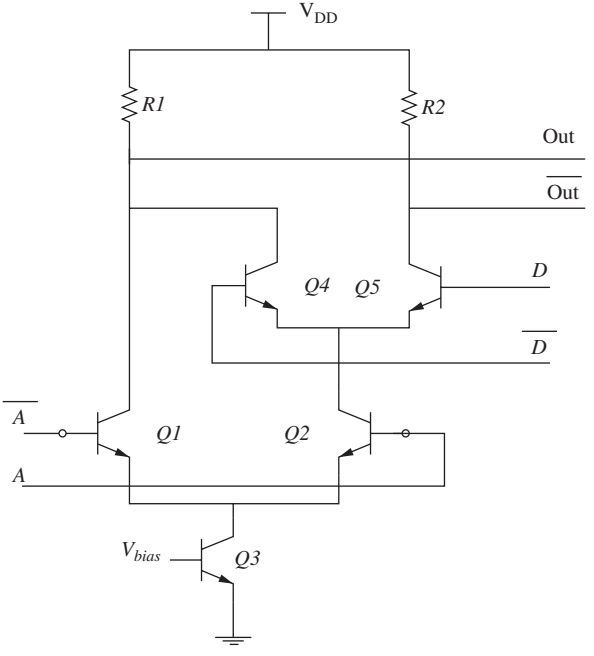


Figure 3-35 NAND circuit schematic

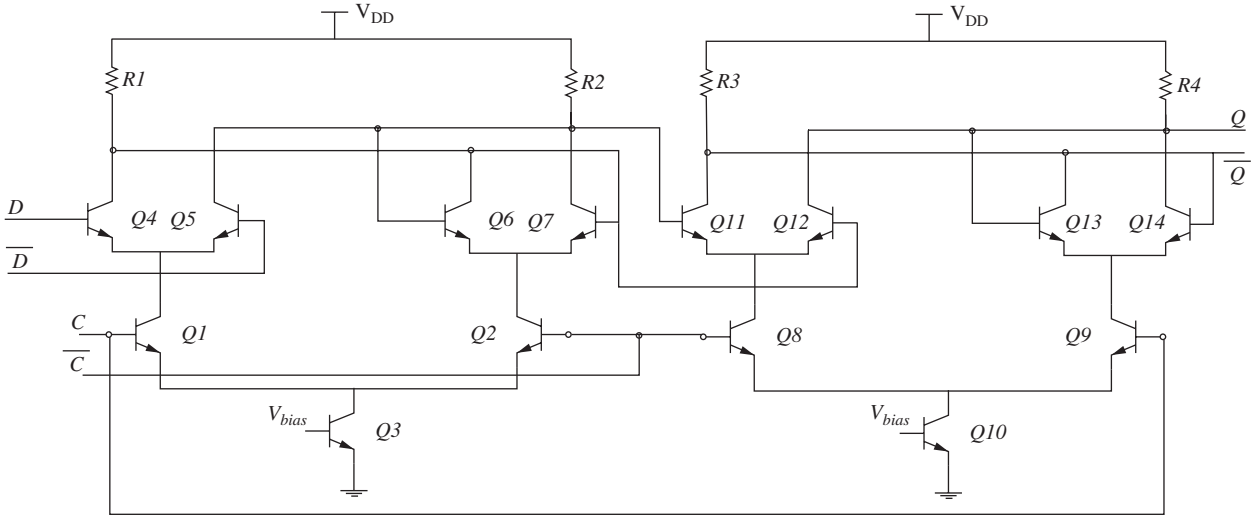


Figure 3-36 D flip-flop circuit schematic

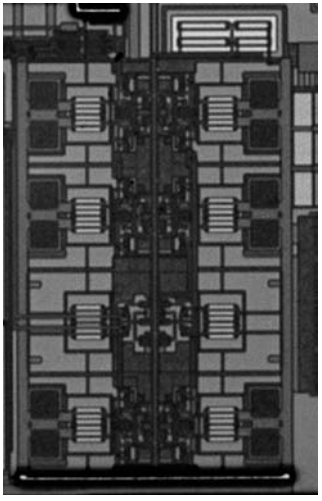


Figure 3-37 Microphotograph of the prescaler

Table 3-13 shows the post-layout results for the two possible settings of the prescaler in regards to the output frequency and the current consumption. Figure 3-38 shows the input and output signals of the prescaler. The input signal is a sinusoidal signal at a frequency of 1.575GHz and the output signal frequency is divided either by 4 or 5, depending on the selection pin. The simulation results have revealed that the prescaler is very sensitive to power supply and ground noise. Therefore, non-ideal ground and a noisy power supply have been included at the simulation stage, and large coupling capacitors have been placed between V_{DD} and GND. Moreover, the delays have been minimised with short connection paths and small area components to minimise the parasitic capacitances.

3.6.2.2 Comparator To convert the output ECL signal from the prescaler to a CMOS logic signal for the digital divider input, an interface is required. The output frequency for the prescaler is around 350MHz, with an amplitude of 250mV peak to peak and a DC voltage of 3.17V (see Figure 3-38). The CMOS logic-required signal is a square signal centred in 1.65V with a 3.3V peak-to-peak amplitude voltage.

The signal conversion is carried out by the differential comparator shown in Figure 3-39. The resulting consumption of the component is less than 1mA.

TABLE 3-13 Post-layout analysis results for the prescaler

S	Fin	Fout	Current Consumption
0V	1.6GHz	400MHz	967.4μA
3.3V	1.6GHz	320MHz	969.1μA

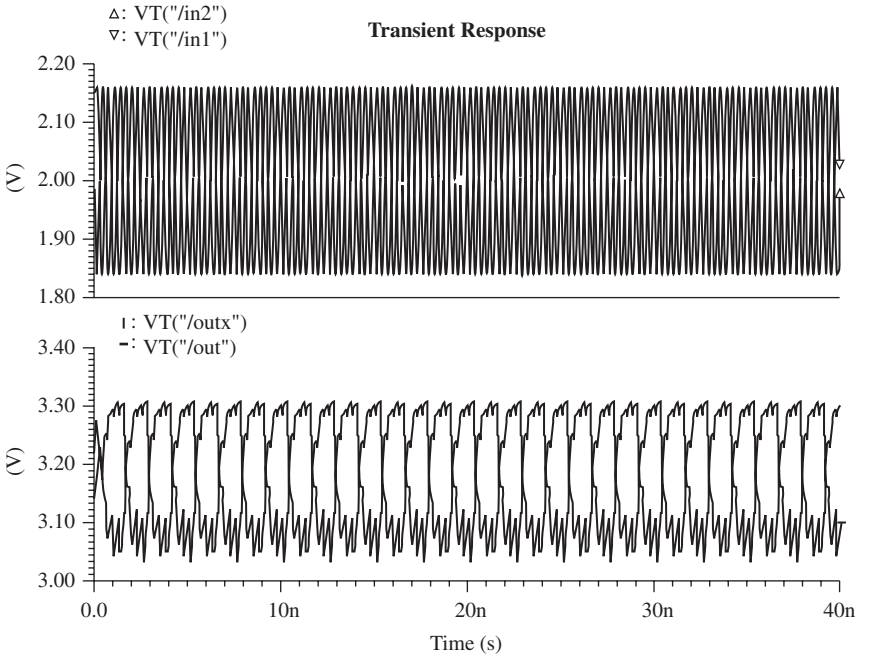


Figure 3-38 Input (top) and output (bottom) signals of the prescaler

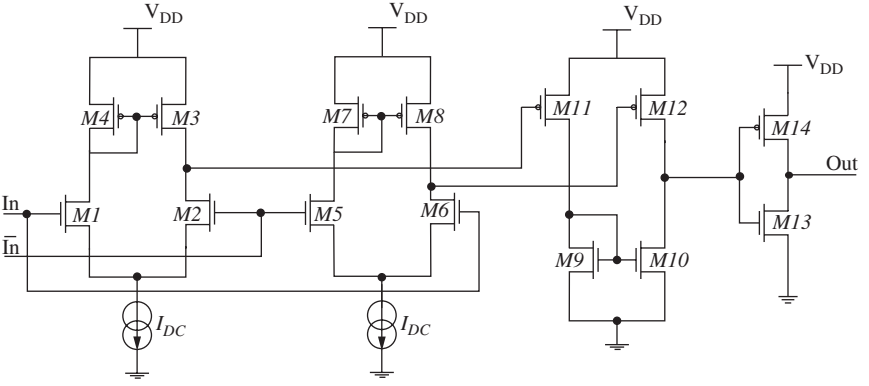


Figure 3-39 Comparator schematic

3.6.2.3 Digital Divider The digital divider consists of a program counter, a swallow counter, and a reset. The working frequency range of the input signals is between 315MHz and 393MHz. The output frequency is 16.368MHz and is compared with the *Xtal* reference frequency. The block diagram is shown in Figure 3-40.

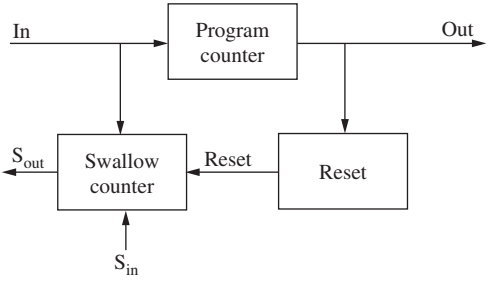


Figure 3-40 Block diagram of the digital divider

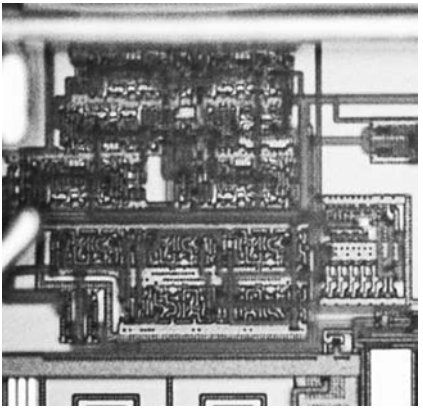


Figure 3-41 Layout of the digital divider

The current consumption of the digital divider, depending on the division ratio, is 852μA for $S = 3V$ and 883μA for $S = 0V$. Figure 3-41 shows the layout with an area of 74×100μm^2. Special attention has been paid to the swallow counter design to minimise gate delays, as an erroneous output signal frequency could result in a divider malfunction. Therefore, a careful layout has been performed to connect different gates to minimise parasitic capacitances caused by signal tracks.

3.6.3 Phase Frequency Detector and Charge Pump

The output of an ideal PFD and charge pump is a current linearly proportional to the phase difference of the inputs, that is, the *Xtal* reference and the PLL feedback loop signal. Eq. 3-39 predicts the ideal behaviour of the PFD and charge pump illustrated in Figure 3-42.

$$I_{out} = K_{PD}\Delta\phi \tag{3-39}$$

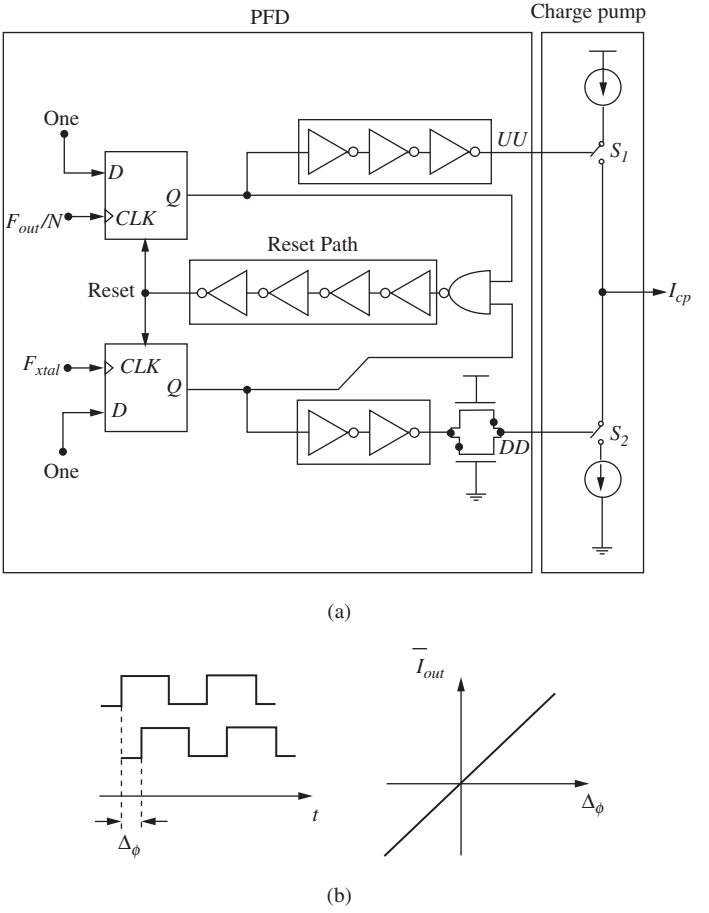


Figure 3-42 (a) Block diagram of a PFD and charge pump; (b) characteristic of an ideal PFD and charge pump

where K_{PD} is the PFD gain [A/rad] and $\Delta\phi$ is the input phase difference. Actually, the performance of the PFD is nonlineal and K_{PD} depends on the amplitude or the duty cycle of the inputs.

The basic PFD consists of two D flip-flops and one AND gate, as shown in Figure 3-42. Depending on which input is high, the corresponding output will be also high; when both outputs are high, the flip-flops are reset. Thus, depending on the frequency difference, one output or the other will be high.

The charge pump consists of an NMOS transistor (*M1*), a PMOS transistor (*M2*), and two current sources (*M3-M13*) (see Figure 3-43).

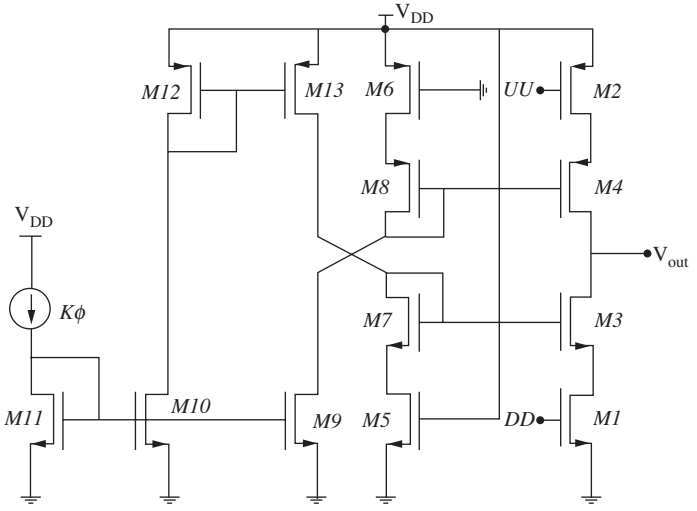


Figure 3-43 Charge pump

Transistors *M1* and *M2* work as switches commuting the two equal current sources. If the up pulse (UU) is longer than the down pulse (DD), the former will be connected longer and current will flow to the loop filter capacitor. In a similar fashion, when the down pulse is longer than the up pulse, voltage will be decreased by means of the current sink, discharging the capacitor. In this manner, input phase difference is amplified by means of a change in the voltage control of the VCO. PFD gain (K_{PD}) is the charge pump current to the 2π (1 cycle) ratio.

One of the drawbacks of this architecture is the dead zone. The *dead zone* is the phase difference between the PFD inputs that keep the charge pump (CP) from injecting or sinking current from the loop filter.

Figure 3-44 shows how, for phase differences below ϕ_0, the current from the charge pump is zero. This effect increases the *jitter* at the

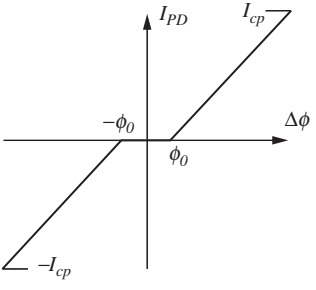


Figure 3-44 Dead zone effect of the PFD/CP

output of the feedback loop, which produces an increase of the phase noise at the output of the PLL.

This effect happens for small phase differences in the inputs when the output pulses of the PFD are not wide enough to activate the charge pump. The most common method to eliminate the dead zone is the placement of an even number of inverters in the reset path (see Figure 3-42(a)), which introduces a delay big enough to activate the charge pump. Therefore, in the locked condition ($\Delta\phi = 0^{o}$), both outputs of the PFD (UU and DD) send pulses to the charge pump of equal width and amplitude. These pulses inject to and sink from the loop filter the same amount of current. As a consequence, the dead zone is eliminated without modifying the VCO control voltage. The minimum delay to be added has been estimated as the average of the up and down time pulses at UU and DD[Lee02].

It is also important to mention that to reduce the level of the spurious, the absolute value of the source and sink current sources should be as equal as possible[Razavi01].

Figure 3-45 shows the post-layout simulation of the output of the PFD. It shows the correct operation of the component with a current consumption of 27μA.

Figure 3-46 shows the output current and voltage of the charge pump. It can be seen how output voltage is increased and decreased depending on whether the current source switch is on or the current sink switch is on. The switches are controlled by the PFD output voltage.

3.6.4 Pierce Oscillator

The crystal oscillator provides the reference signal to the PFD and the clock signal to the ADC and the digital circuitry.

Figure 3-47 shows the architecture selected for the pierce oscillator; the components inside the square have been integrated in the chip.

R_{bias} is a feedback resistance providing DC bias for the inverter amplifier. C_1 and C_2 are the capacitors of the quartz crystal load and set the oscillating frequency together with the quartz crystal. R is the resistor employed to minimise the current flowing through the quartz.

The quartz crystal can be modelled electrically, as shown in Figure 3-48. C_p is the total capacitor between terminals, L_s is the vibrating mass of the crystal, and C_s is its elasticity. R_s represents the losses associated with the crystal. The output frequency depends on these values.

The standard characteristics of a crystal are shown in Figure 3-49.

The series resonance frequency is defined by Eq. 3-40, which is solely determined by the motional parameters of the crystal, L_s and C_s. The parallel resonance is higher than the series resonance and is defined

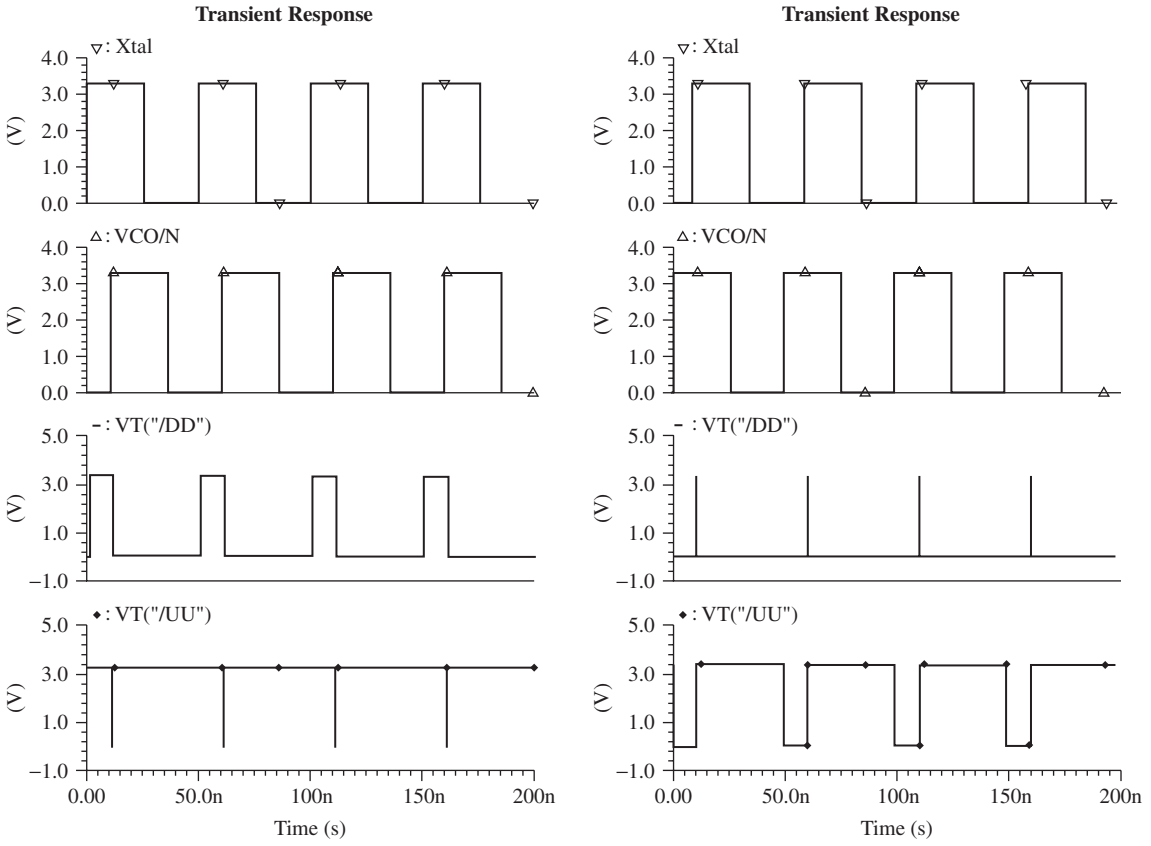


Figure 3-45 PFD input and output signals for $\Delta\phi = \pm 10$ns. From the top to the bottom: *Xtal*, VCO/N, DD, and UU pulses.

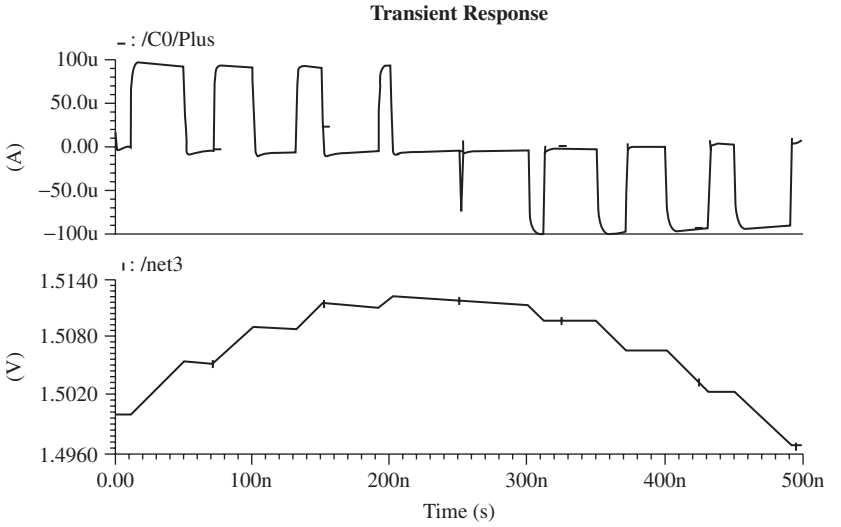


Figure 3-46 Output voltage and current of the charge pump obtained from the post-layout simulation

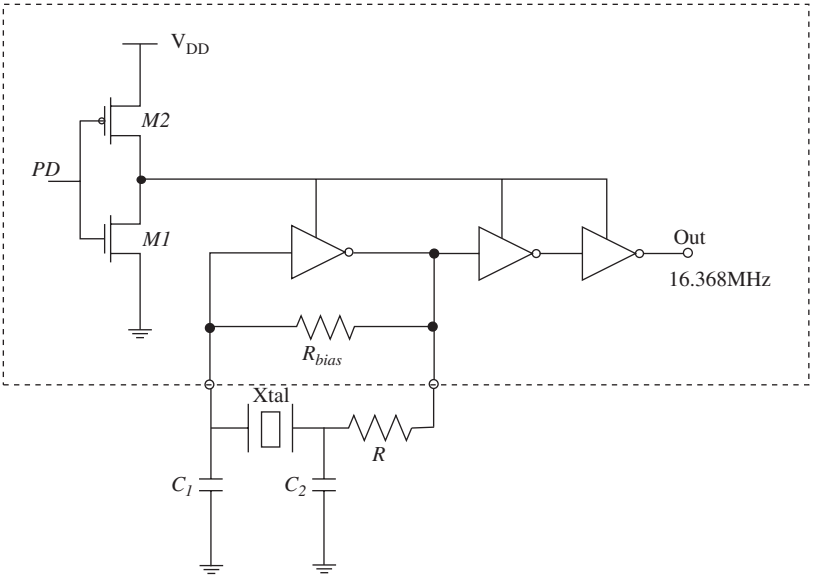


Figure 3-47 Pierce oscillator

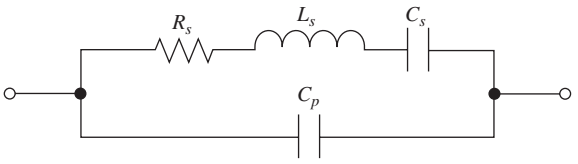


Figure 3-48 Quartz crystal equivalent circuit

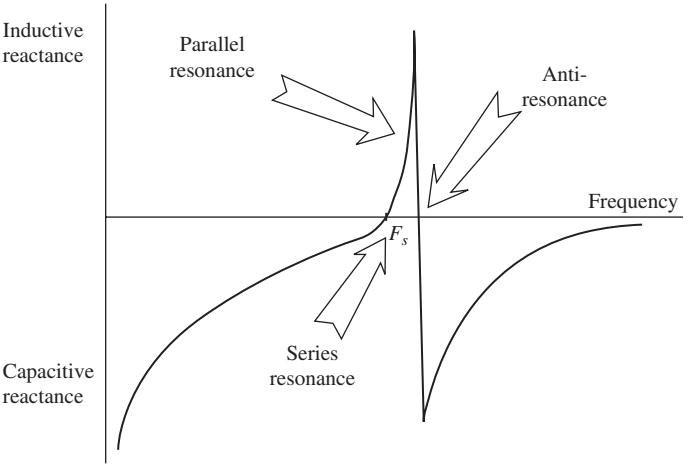


Figure 3-49 Reactive characteristics of the quartz

by Eq. 3-41 where Eq. 3-42 is as shown. The selected configuration makes the crystal work at the parallel resonance frequency.

$$F_{series} = \frac{1}{2\pi\sqrt{L_s \cdot C_s}} \tag{3-40}$$

$$F_{parallel} = F_{series}\left(1 + \frac{C_s}{2C_{eq}}\right) \tag{3-41}$$

where

$$C_{eq} = C_p + C_1\left(\frac{C_2}{C_1 + C_2}\right) \tag{3-42}$$

To ensure oscillation, Barkhausen criteria has to be fulfilled, which defines that the gain must be higher than one and the phase must be equal to 0º. The inverter amplifier simultaneously provides a gain

higher than one and a phase of 180º. Therefore, C_1 and C_2 capacitors provide another 180º to reach 0º[EXARDAN108]. To produce oscillation at the nominal frequency, the value of the capacitors has to be the same as the load capacitor (Eq. 3-43) given by the manufacturer. The remaining two inverters work solely as buffers.

$$C_L = \frac{C_1 \cdot C_2}{C_1 + C_2} \tag{3-43}$$

The values of the components considered in the simulation are summarised in Table 3-14. For capacitors C_1 and C_2, parasitic resistance and inductance are also included. For these parameters, the oscillation is obtained with a current consumption of 0.7mA. The layout of the oscillator is shown in Figure 3-50.

TABLE 3-14 Values of the parameters of the pierce oscillator for the simulation

Parameter	Value	Parameter	Value	Parameter	Value
C_s	140.4fF	R_{bias}	100kΩ	C_1,C_2	56pF
R_s	20Ω	R	1.2kΩ	L_1,L_2	910pH
L_s	679.7µH			R_1,R_2	0.181Ω
C_p	7pF				

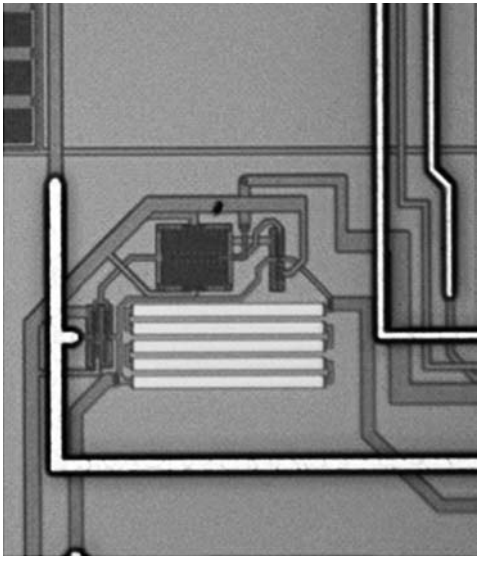


Figure 3-50 Microphotograph of the pierce oscillator

3.6.5 Loop Filter

The use of passive filters over active filters in today's high-performance digital PLL is recommended due to passive filters' lower noise and complexity. The basic passive filter configuration for a current mode charge pump PLL, such as the one described in the previous sections, is shown in Figure 3-51(a). The loop filter is a complex impedance in parallel with the input capacitance of the VCO. The PFD's output signals control the charge pump current within the loop filter, which then converts the current into the VCO's control voltage. An extra-low pass filter section sometimes is needed to provide additional rejection of the reference sidebands, known as spurious. Figure 3-51(b) shows a third-order passive filter where a low-pass filter section ($R3$ and $C3$) has been added at the output.

Table 3-15 shows the transfer function ($Z(s) = I_{in}(s)/V_{out}(s)$) of the second- and third-order passive loop filters. The filter component values can be determined from the open loop gain bandwidth (ω_p), the phase

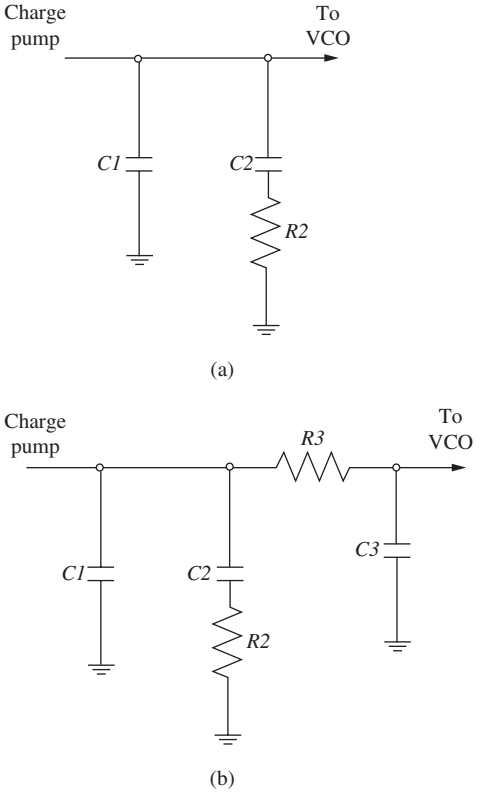


Figure 3-51 Passive loop filters: (a) second order and (b) third order

TABLE 3-15 Transfer functions and different equations to determine the filter component values of the second- and third-order passive loop filters

	Second Order	Third Order
T1	$\frac{1/\cos\phi_p - \tan\phi_p}{\omega_p}$	$\frac{1/\cos\phi_p - \tan\phi_p}{\omega_p}$
T2	$\frac{1}{T1\cdot\omega_p^2}$	$\frac{1}{(T1+T3)\cdot\omega_c^2}$
T3	—	$\sqrt{\frac{10^{ATTEN/20}-1}{(2\cdot\pi\cdot F_{ref})^2}}$
ω_0	ω_p	$\frac{\tan\phi_p\cdot(T1+T3)}{(T1+T3)^2+T1\cdot T3}\cdot\left[\sqrt{1+\frac{(T1+T3)^2+T1\cdot T3}{(\tan\phi_p\cdot(T1+T3))^2}}-1\right]$
C1	$\frac{T1}{T2}\cdot\frac{K_\phi\cdot K_{VCO}}{\omega_p^2\cdot N}\sqrt{\frac{1+(\omega_p\cdot T2)^2}{1+(\omega_p\cdot T1)^2}}$	$\frac{T1}{T2}\cdot\frac{K_\phi\cdot K_{VCO}}{\omega_c^2\cdot N}\cdot\sqrt{\frac{1+(\omega_c\cdot T2)^2}{(1+(\omega_c\cdot T1)^2)\cdot(1+(\omega_c\cdot T3)^2)}}$
C2	$C1\cdot\left(\frac{T2}{T1}-1\right)$	$C1\cdot\left(\frac{T2}{T1}-1\right)$
C3	—	$\le\frac{C1}{10}$
R2	$\frac{T2}{C2}$	$\frac{T2}{C2}$
R3	—	$\frac{T3}{C3}$
Z(S)	$\frac{1+s\cdot C2\cdot R2}{s\cdot(C1\cdot C2\cdot R2\cdot s+C1+C2)}$	$\frac{\frac{Z_{2^{o}Orden(s)}}{s\cdot C3}}{Z_{2^{o}Orden(s)}+R3+\frac{1}{s\cdot C3}}$

margin (ϕ_p), the added attenuation from the output low-pass filter section (*ATTEN*), the *Xtal* reference frequency (F_{ref}), the main divider ratio (N), the phase detector/charge pump constant (K_ϕ), and the voltage-controlled oscillator-tuning voltage constant (K_{VCO}),[Kee96].

In Table 3-15, $T1$, $T2$, and $T3$ are the time constants that determine the two poles and one zero frequencies, respectively; s is the complex

TABLE 3-16 Calculated and standard values of the loop filter

Parameter	Simulation	Standard	Unit
C1	659	680	pF
C2	3.27	3.3	nF
C3	65	68	pF
R2	3.141	3	KΩ
R3	813	750	Ω

variable; ω_p and ω_c are the frequencies where the open loop gain of the second- and third-order filters respectively are 0dB; and $Z_{2^oOrden(s)}$ is the transfer function of the second-order passive filter.

In the design example, a third-order passive loop filter has been selected. Locating the point of minimum phase shift at the unity gain frequency of the open loop response ensures loop stability. The phase relationship between the first pole and the zero also allows easy determination of the loop filter component values, as shown in Table 3-15. The phase margin (ϕ_p), defined as the difference between 180º and the phase of the open loop transfer function at frequency ω_p, has been set to 48º. In this manner, an optimum trade-off between loop stability, attenuation of F_{ref}, and loop response has been achieved.

Notice that, to attenuate the spurs, the frequency of the additional pole introduced by the output low-pass section is lower than F_{ref}. However, it is higher than the loop bandwidth so as not to compromise loop stability.

Table 3-16 shows the values of loop filter components obtained from the previous equations and the ones matched to the standard values available on the market.

3.7 Overall Considerations

This section presents the designed control logic that allows for different working modes by means of three additional control pins. It can switch the entire receiver on or off or switch on only the pierce oscillator and digital buffers of the RF front-end, creating only the clock for the digital IC.

Some considerations about the floor planning of the entire front-end are also presented in this section, which is a key element in the successful completion of the receiver. The location and interconnections of all the blocks have to be carefully designed. The different PADs used in the design, along with their purposes, are also described in this section.

Finally, the necessary external components, such as the antenna, SAW filters, and so on, are listed.

3.7.1 Operation Modes of the Front-End

To control the receiver and switch it on and off, three input pins have been defined: two CE (chip enable), CE1 and CE2; and an FS (frequency selection). The logical gates utilised to implement the CE function are shown in Figure 3-52. Four different operation modes can be set using the CE pins (see Table 3-17).

These modes allow the receiver to be switched off (first mode) and the pierce oscillator and the digital output buffers of the RF front-end to be switched on, powering only the clock for the digital IC (third mode). Hence, the RF front-end can be set to stand-by mode when required by the digital IC, minimising power consumption. These modes also allow the complete receiver to be switched on (fourth mode). This is the normal mode of operation. In all the previously mentioned operation modes, the frequency selection pin selects the LO frequency. However, in the second mode of operation, known as test mode, the FS pin allows the current of the different blocks of the entire receiver to be controlled. This way, by means of the intermediate PADs, separate testing of each part of the chip is possible.

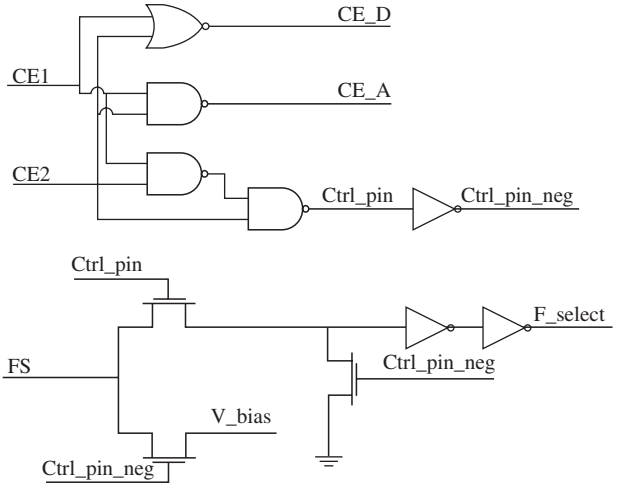


Figure 3-52 CE gate diagram

TABLE 3-17 Front-end operation modes

CE1	CE2	FS	F_select	CE_D	CE_A	V_bias	Mode
0	0	0 1	0 1	1	1	—	Off
0	1	V_bias	0	0	1	V_bias	Test Mode
1	0	0 1	0 1	0	1	—	Digital On-Analogue Off
1	1	0 1	0 1	0	0	—	Digital On-Analogue On

3.7.2 Floor Planning and Chip Layout Considerations

Figure 3-53 shows the microphotograph of the entire RF front-end chip. The chip size is approximately 2800×3000μm^2 and it is a PAD-limited design. Due to the high frequency of the incoming signal, many layout issues may affect the performance of the receiver. These may include, for example, coupling through the substrate, placing components and PADs, and so on.

Much attention has been given to these issues during the placement of the different blocks. The PLL is placed at the top-left and the RF mixer at the bottom-left. The LNA is placed at the bottom-right, far away from the noisy pulse swallow divider of the PLL. In this manner, the performance of the LNA is not degraded. All signal PADs are placed between AC ground PADs. All PADs are installed by stacking metal layers from metal 1 to metal 4, except for RF PADs, where only metal 4 has been used in order to reduce the PAD parasitic capacitance. All PADs are also electrostatic discharge (ESD)-protected. RF pads are installed using an analogue ESD-protection circuit with a very low and almost constant input capacitance, high-ESD level, and no series resistance[Ming-Dou02]. This was done to minimise performance degradation of the front-end due to the ESD protections. The performance of the implemented ESD structures are 2kV for the HBM standard and 300V for the MM standard. Figure 3-54 shows the implemented RF ESD

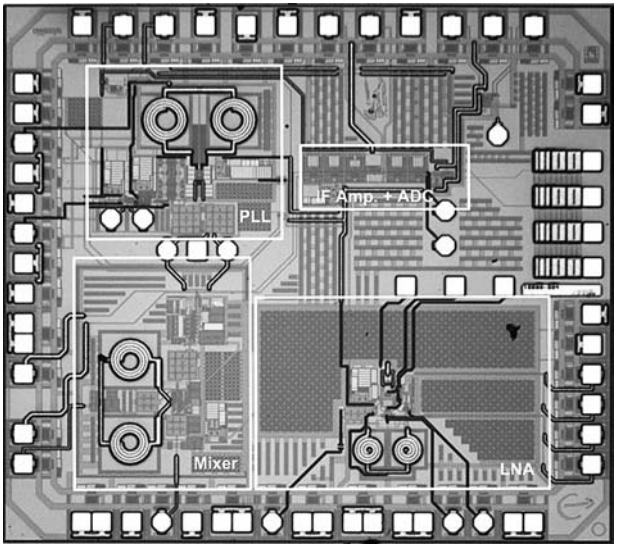


Figure 3-53 GPS and Galileo RF Front-End IC microphotograph

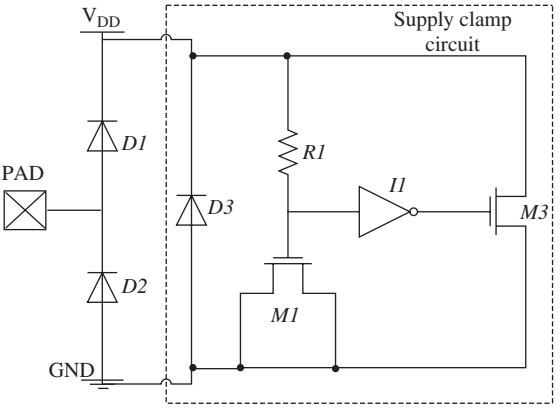


Figure 3-54 ESD-protection circuit for analogue PADs

protection with the input diodes and the clamping circuit. Digital PADs are employed with standard ESD-protection circuits coming from the input/output (I/O) cells supplied by the foundry. Analogue and digital grounds are also isolated. Large substrate contacts and guard rings separate the different blocks to prevent parasitic coupling. A symmetric layout has been performed in each component (LNA, RF mixer, PLL, etc.) to keep the signal path truly differential. This allows the effect of the voltage supply and ground parasitics to be minimised and the harmonic distortion of the VCO to be reduced. Special attention has been paid to the LC tank layout to minimise the parasitic resistance and capacitance of the connection tracks. A careful layout is also required for the pulse swallow divider and the prescaler, to reduce the signal delay in their feedback loops.

The chip has been packaged in a commercial plastic TQFP 48-pin package. The description for the pins is shown in Table 3-18 and Figure 3-55. Different power supplies and ground pins are specially made for the different parts of the front-end. This has been done to avoid noise coupling among all of them, especially between the sensitive RF blocks, such as the LNA, and the digital noisy blocks, such as the clock output buffers or PLL divider. This is also suitable for testing the final chip. Thereby, 10 pins are located for voltage supply: V_{DD}_IF, V_{DD}_LOGIC2, V_{DD}_BUFFER, V_{DD}_LOGIC, V_{DD}_LNA, V_{DD}_RF, V_{DD}_VCO, V_{DD}_PRE, V_{DD}_LOGIC, and V_{DD}_XTAL. Regarding the ground pins, there are 16: two for GND_IF, GND_LOGIC2, GND_BUFFER, and GND_LOGIC; three for GND_LNA; two for GND_RF; four for GND_PLL; and two for GND_XTAL. There are two internal grounds: one analogue and one digital. As presented in Figure 3-56.

TABLE 3-18 Front-end IC pins and description

PIN	Symbol	Description
1	V_{DD}_XTAL	Power supply
2	V_{DD}_LOGIC	Power supply
3	LF_2	Loop filter
4	V_{DD}_PRE	Power supply
5	GND	Ground
6	LF_1	Loop filter
7	V_{DD}_VCO	Power supply
8	GND	Ground
9	GND	Ground
10	IF+	Mixer output
11	IF–	Mixer output
12	GND	Ground
13	GND_RF	Ground
14	RF_IN+	RF amp. input
15	RF_IN–	RF amp. input
16	GND_RF	Ground
17	V_{DD}_RF	Power supply
18	LNA_OUT	LNA output
19	GND_LNA	Ground
20	V_{DD}_LNA	Power supply
21	GND_LNA	Ground
22	LNA_IN+	LNA input
23	LNA_IN–	LNA input
24	GND_LNA	Ground
25	GC	LNA gain control
26	AS_OUT	Antenna sensor output
27	AS_2	Antenna sensor input
28	AS_1	V_{DD} antenna supply
29	V_{DD}_LOGIC	Antenna power supply
30	GND_LOGIC	Ground
31	V_{DD}_BUFFER	Power supply
32	GND_BUFFER	Ground
33	DATA	Data
34	CLOCK	Clock
35	GND_LOGIC2	Ground
36	V_{DD}_LOGIC2	Power supply
37	CE2	Chip enable (no data)
38	CE1	Chip enable

TABLE 3-18 Front-end IC pins and description (*continued*)

PIN	Symbol	Description
39	F_SELECT	Frequency selector
40	GND_IF	Ground
41	IF–	Limiting amp. output
42	IF+	Limiting amp. output
43	GND_IF	Ground
44	V_{DD}_IF	Power supply
45	GND_XTAL	Ground
46	XTAL_IN	Crystal input
47	XTAL_OUT	Crystal output
48	GND_XTAL	Ground

Figure 3-56 the RF amplifier mixer and the LNA ground and supply pads use double bonding to reduce parasitic bondwire inductance and improve stability of the RF amplifiers. Three pins have been defined for the control logic, as shown in the previous section. The rest of the pins (17) are input or output pins related to the signal path, crystal, and

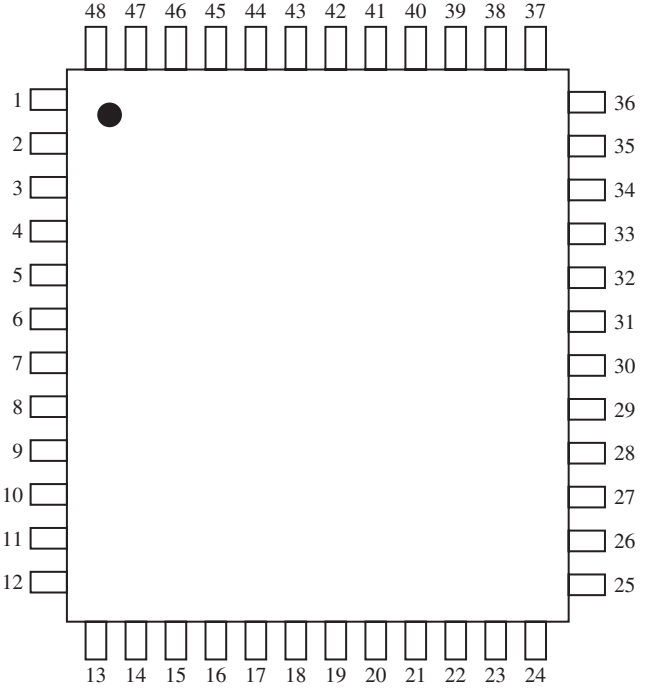


Figure 3-55 Pin package layout

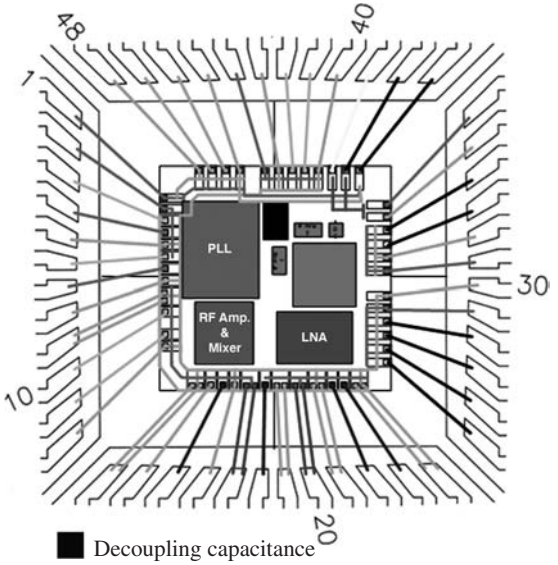


Figure 3-56 Floor-planning and bonding diagram

loop filter of the PLL, and gain selection pins for the LNA. The input signal of the receiver is a single-ended signal at LNA_in+ (LNA_in– is connected to an AC ground through a capacitor), while the outputs of the front-end are the navigation DATA and CLOCK.

Moreover, intermediate pads have been included in the design to check different points of the front-end. Measurement of some components of the circuit separately can be carried out with the test mode available. In this way, the designer can save time and money, as one design can validate the different parts and the whole as one.

3.7.3 External Components

Although the design of the front-end is considered highly integrated, some external components are required, apart from coupling and decoupling capacitors or impedance-matching inductors and capacitors. The required external components include the antenna, the 16.368MHz quartz crystal (TCXO), RF SAW filters, IF filters, and the loop filter.

The antenna can be either active or passive. The RF SAW filters are located between the LNA and the down-conversion stage and optionally between the antenna and the LNA. The target is to block adjacent jamming signals that could compromise the performance of the front-end.

The design example utilises the Murata RF SAW filters DFCB21G57LDJAB-TT1 next to the antenna and the NSVA352 from the NJR Corporation between the LNA and the down-conversion stage.

3.8 Summary

The circuit design flow of a GPS and Galileo front-end has been explained and a design example has been successfully carried out. The designs and post-layout simulation results of every block of the front-end have been presented. Some specifications, such as the gain of the LNA, have not been met. However, this has been compensated for by other blocks such as the IF, which has a higher gain than specified. Moreover, estimated input offset of the ADC during the system analysis was four times higher than the simulated one. Therefore, less stringent specifications could be applied to the design.

The proposed floor-planning minimises the RF signal path length and the coupling between the critical blocks. In addition, 48 pads are defined and located for the packaging of the entire front-end. Moreover, ESD protections have been added to the design and the control logic has been defined to control the various operations of the front-end. Finally, required external elements such as RF SAW filters have been selected.

Chapter

4

Measurements

Once the design and fabrication of the receiver have been carried out, validation is required. This chapter deals initially with the characterisation of the blocks and finally with the measurement of the whole front-end. The different test setups used are described with this objective in mind. Moreover, the required printed circuit board (PCB) and external components are also presented. Finally, the performance of the entire front-end is compared with that of a commercial one.

4.1 Introduction

When it comes to the characterisation of an integrated circuit (IC), it is mandatory to distinguish two stages: the test stage dedicated to the validation of the design, and the post-fabrication test stage that ensures the level of quality of the product.

This chapter is dedicated to the first of the aforementioned stages, within which the following points will be described: on-wafer measurement techniques for passive elements, and testing techniques for both the different blocks of an encapsulated integrated circuit and the whole receiver chain.

4.2 Stages in the Validation of an Integrated Circuit Design

Multiple factors play a major role in the design of an integrated radio frequency (RF) front-end. Some of them are difficult to quantify and poorly described in industry literature. If these factors are not correctly considered, inefficient and expensive redesign loops may result, making the design of an IC unfeasible.

These factors include:

- Accurate models of the passive elements included within the integrated circuit in the frequency range where they are expected to work Integrated inductors, varactors and RF pads with electrostatic discharge (ESD) protections are key elements to take into account.
- The influence of the substrate on the performance of the different blocks of the IC. For example, the substrate noise coupling in the integrated spiral inductors and varactor of a voltage controlled oscillator (VCO) will degrade the phase noise performance of the local oscillator. In a similar way, the noise coupled through the substrate to the inductors of the low-noise amplifier (LNA) will increase the noise figure.
- The influence that the different blocks encapsulated in the same package have on each other. For example, the current peaks required by the digital part of the local oscillator may couple through the power supply bondwires to the VCO and cause spurious tones in the phase noise response.
- Influence of the bondwires. Underestimation or overestimation of the parasitic inductance associated with the bondwires may result in either a decrease or an increase in the gain of the single-ended stages.

To identify whether or not a design fails due to one of the previously mentioned factors, designers must establish a methodology to validate the design throughout several stages. The stages to be completed are:

- Validation of the models of the integrated passive elements when not provided by the foundry.
- Validation of the blocks that compose the RF front-end separately.
- Validation of the blocks interacting with other blocks of the RF front-end.
- Validation of the whole RF front-end.

4.3 Validation of Passive Element Models

Typically, foundries do not provide accurate models of passive elements for RF applications. Their models tend to leave out the following:

- Inductors
- Varactors
- RF pads with ESD protections

The rest of the components of the integrated circuits (transistors, resistors, capacitors, etc.) are usually correctly modelled by the foundry and the data provided can be considered reliable.

Having a reliable model of these components should be considered essential prior to the design of the RF front-end blocks, such as the LNA and VCO.

An incorrect modelling of the integrated inductors may incur:

- Divergences between the simulated and the measured linearity, gain, and noise figure in the LNA block.
- Divergences among the phase noise, oscillation frequency, output power, and tuning range in the VCO block.

An incorrect modelling of the varactor may create divergences in the phase noise, oscillation frequency, output power, and tuning range in the VCO block.

An incorrect modelling of the RF pads with ESD protection may cause an important increase in the noise figure (NF) and an input impedance mismatch in the LNA.

The passive components should be measured on-wafer. The measurement process is widely detailed in [Aguilera03] and [Gutierrez07]. The necessary steps to be taken are briefly summarised as follows:

1. Design the measuring structure for the passive element (see Figure 4-1).
2. Design the de-embedding structure that eliminates the influence of the measuring structure from the passive element itself (see Figure 4-2).

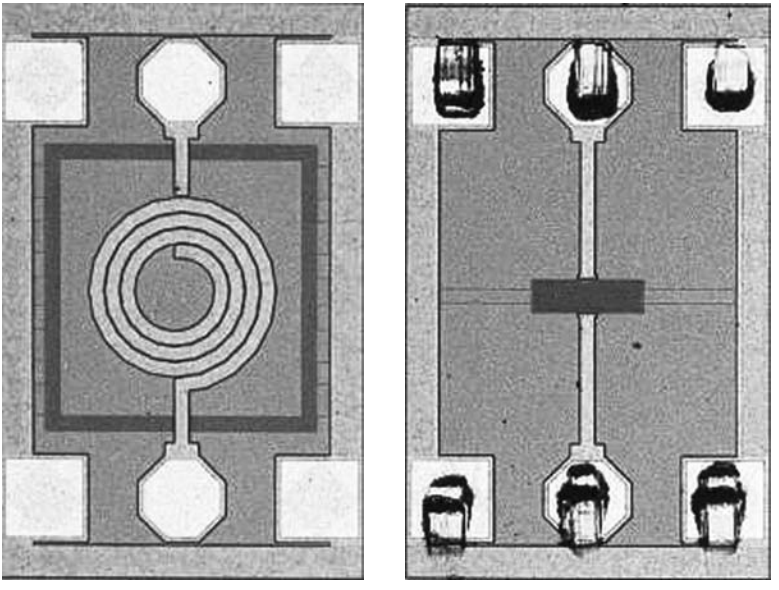


Figure 4-1 Microphotograph of the integrated inductor (left) and varactor (right) inside the measurement structure

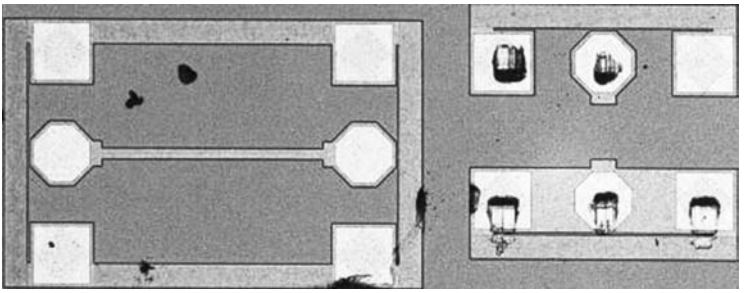


Figure 4-2 Microphotograph of the de-embedding structure for the integrated inductor and varactor

Figure 4-3 Photograph of the on-wafer test setup

3. Test setup calibration (see Figure 4-3).
4. Measure the passive element embedded in the measuring structure.
5. Measure the de-embedding structures.
6. Perform the data processing necessary to de-embed the passive element from the measuring structure.
7. Identify the electric model that describes the response of the passive element in the frequency range of interest once the influence of the measuring structure has been eliminated.

4.4 Individual Validation of Receiver Chain Blocks

Once the information about the passive elements has been obtained, the design and subsequent fabrication of the entire IC is possible.

The microphotograph of Figure 4-4 presents the complete RF front-end, the design of which is explained in the previous chapter. The main components of this design example can be distinguished: the LNA, mixer,

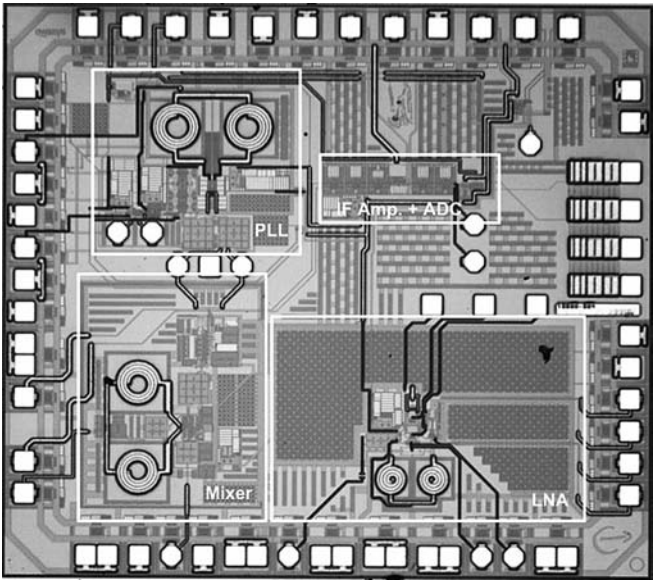


Figure 4-4 Microphotograph of the RF front-end for dual GPS and Galileo

phased-lock loop (PLL), Intermediate Frequency Amplifier (IFA), and analogue-to-digital converter (ADC).

It is worth mentioning that internal pads for the individual validation of the blocks have been specially included.

The IC is encapsulated in a TQFP48 package, mounted on a PCB that contains all the required external components for characterisation, as shown in Figure 4-5. These components include the decoupling capacitors, SAW filters, *Xtal* resonator, matching network, and connectors.

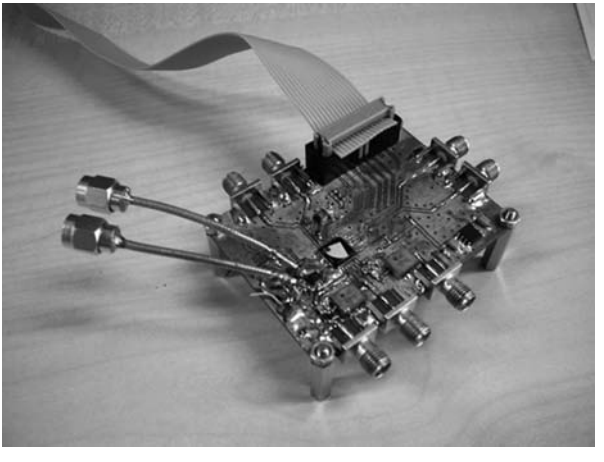


Figure 4-5 Packaged IC mounted on the PCB

Three different PCBs have been designed to characterise the different blocks separately. Thus, three different bonding diagrams for connecting the die to the package have been designed using the intermediate pads. Figure 4-6 illustrates the bonding diagrams.

The diagrams described in Figure 4-6 allow for the separate measurement of the different parts of the RF front-end.

As the bonding diagram in Figure 4-6(a) includes output digital pads and a disconnected PLL, the package pins of these sides can be connected to the intermediate pads located at the mixer LO input and the IF2 output. In this manner, RF and IF amplifiers and mixers can be measured separately from the rest of the front-end. Moreover, the LNA could also be measured with this configuration. However, the configuration shown in Figure 4-6(b) has been used for this approach.

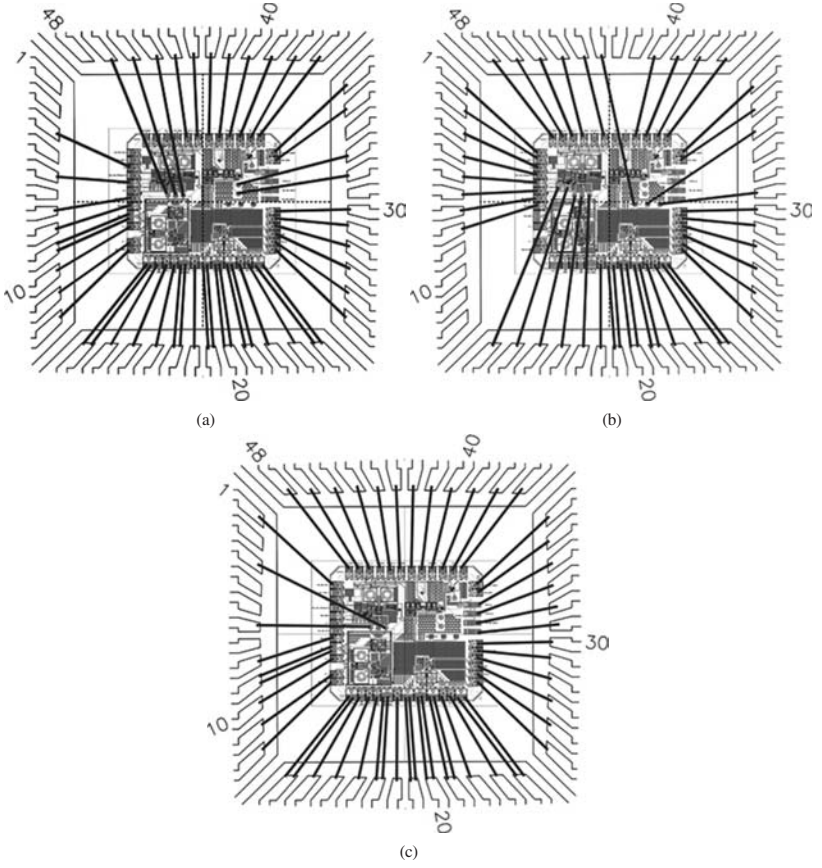


Figure 4-6 Bonding diagrams for the individual characterisation of the receiver chain blocks: (a) test mode chip bonding diagram for measuring the RF amplifier+mixer and the IF amplifier; (b) test mode chip bonding diagram for measuring the LNA and the PLL; (c) test mode chip bonding diagram for measuring the front-end with an external Local Oscillator (LO)

The bonding diagram in Figure 4-6(b) shows the IF amplifier, the RF amplifier, the mixer, and the disconnected digital outputs. Therefore, the intermediate pads of the LNA and the PLL can be connected to the pins of the package. With the intermediate pads of the LNA, the output of the gain selection circuitry can be measured and the current of the LNA can be changed directly. The intermediate pads of the PLL are located at the output of the VCO and between the divider and the phase frequency detector so that the different parts of the PLL can be characterised separately.

Finally, in the bonding diagram shown in Figure 4-6(c), the PLL is not connected, allowing the measurement of the receiver chain with an external LO from the pin connected to the intermediate pads of the VCO output. Moreover, with the test mode of the control logic of the chip, the current of the front-end's components can be modified, adding greater flexibility to the design characterisation.

4.4.1 LNA Measurement

The LNA has been measured on the PCB from the packaged IC with the configuration shown in Figure 4-6(b). This is possible because the LNA is connected to the external SAW, making the input and the output directly available through the IC pins, as shown in Figure 4-4. The packaged LNA has been measured using the test setups described in Figures 4-7, 4-8, and 4-9.

Figures 4-10 and 4-11 show the input and output return loss for the high-gain mode of the LNA measured with the network analyser (Agilent E5071A). Both are below –10dB at the working frequency and therefore meet specifications.

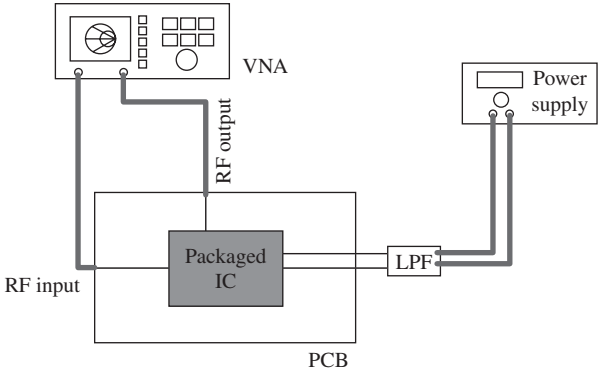


Figure 4-7 Test setup for the characterisation of the gain and return loss of the LNA

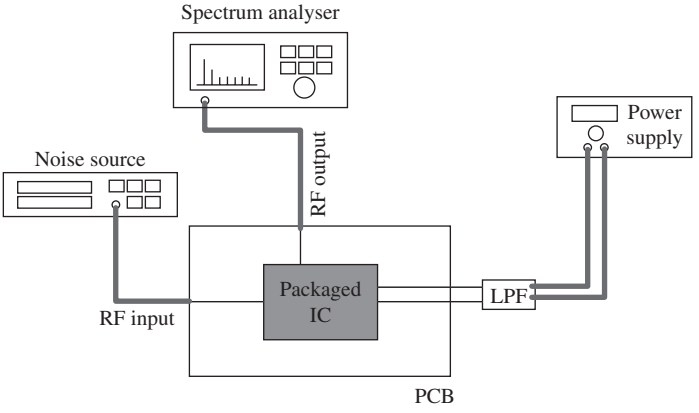


Figure 4-8 Test setup for the characterisation of the noise figure of the LNA

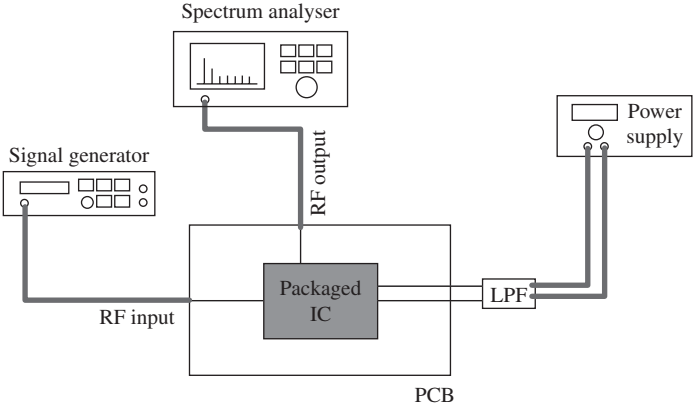


Figure 4-9 Test setup for the characterisation of the 1dB compression point of the LNA

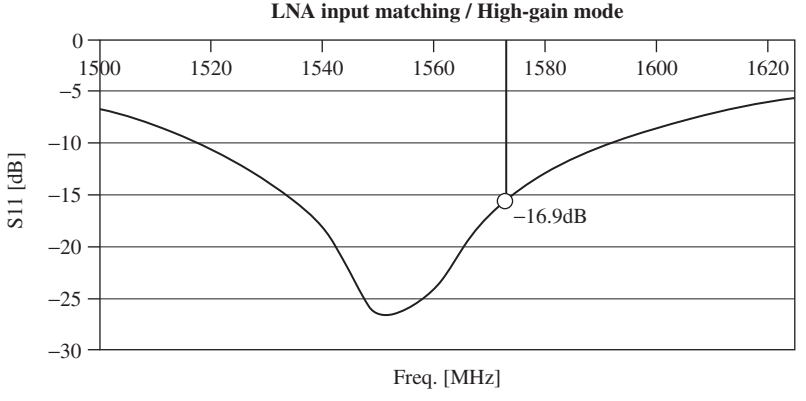


Figure 4-10 LNA high-gain mode return loss

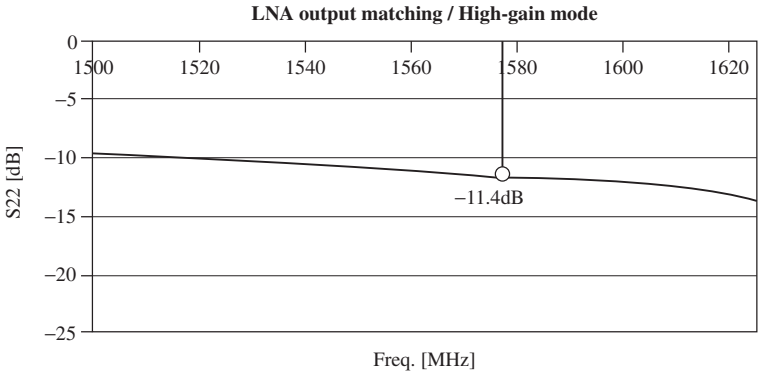


Figure 4-11 LNA high-gain mode output return loss

The external input matching network has been implemented with MURATA components (0603) and is shown in Figure 4-12.

The input impedance matching is worse for low-gain mode than for high-gain mode. However, optimisation in the power transmission is preferred for high-gain mode, as low-gain mode will have an active antenna that will amplify the incoming signal. The input return loss for low-gain mode is shown in Figure 4-13.

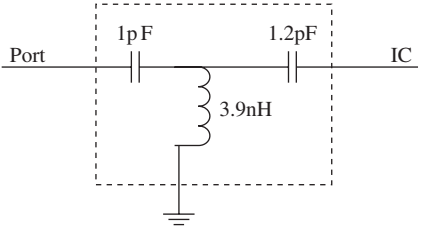


Figure 4-12 LNA input matching network

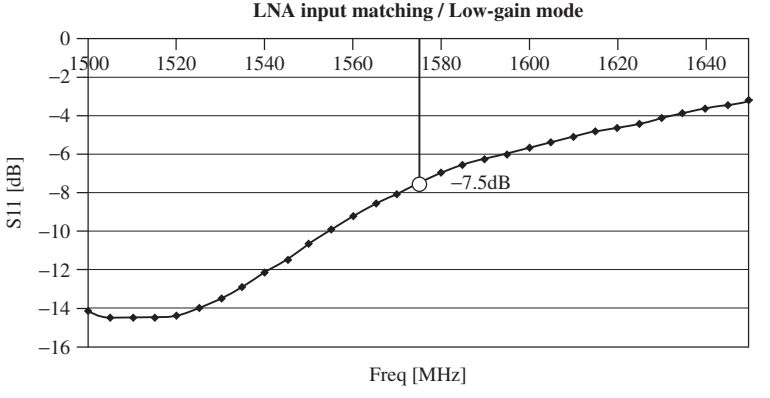


Figure 4-13 Return loss of the LNA in low-gain mode

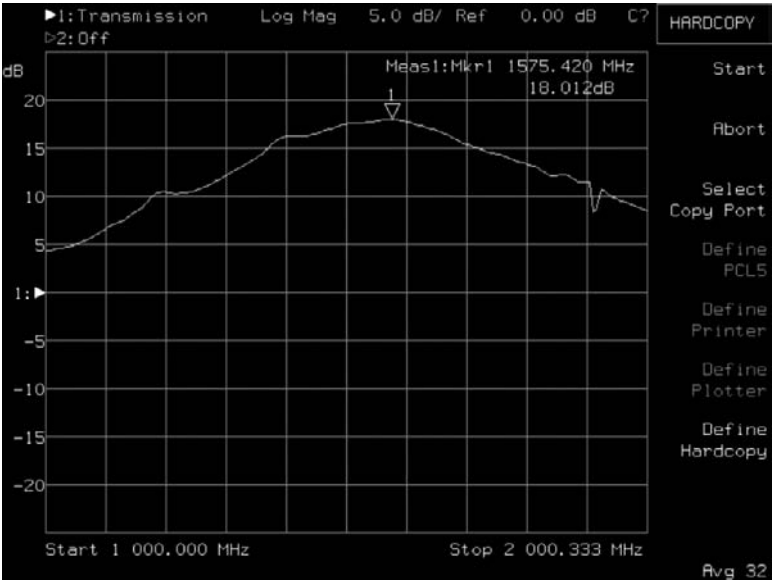


Figure 4-14 Gain of the LNA in high-gain mode

The reading of the VNA (Agilent E5071A) illustrated in Figure 4-14 shows the gain of the LNA in high-gain mode. Moreover, the noise figure for high-gain mode measured with the noise figure spectrum analyser option is shown in Figure 4-15. Additionally, the insertion loss of the SAW filter connected just before the LNA of 0.5dB has to be taken into account.

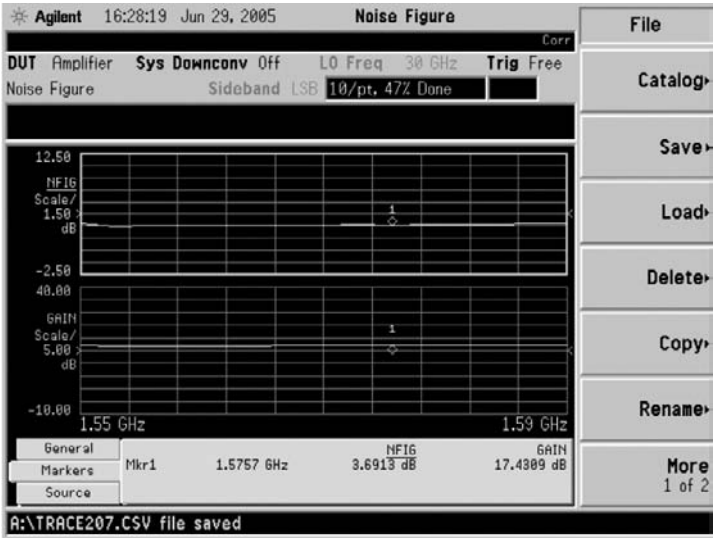


Figure 4-15 Noise figure (upper trace) and gain (lower trace) of the LNA in high-gain mode

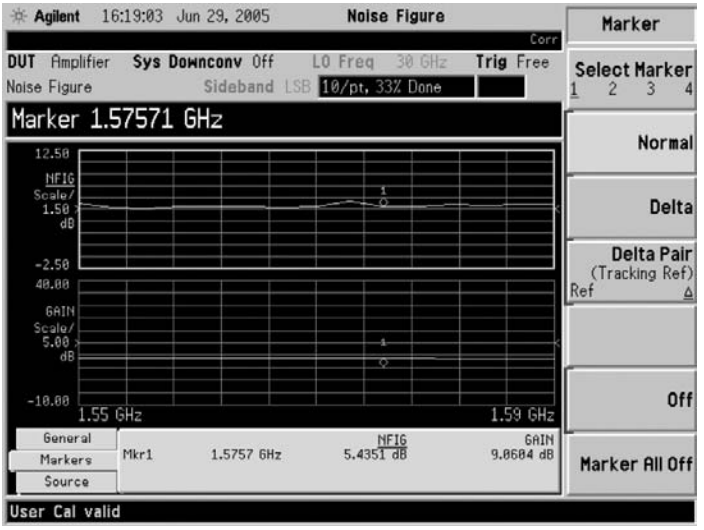


Figure 4-16 Noise figure (upper trace) and gain (lower trace) of the LNA in low-gain mode

Therefore, a gain of 18dB and a noise figure of 3.2dB have been obtained for the LNA. For low-gain mode, as shown in Figure 4-16, the gain is 9.5dB and the noise figure 5dB, after considering the insertion loss of the SAW filter. The noise figure has been measured with the Agilent E4402B spectrum analyser with noise figure measurement option 219 and noise source 346A.

Figure 4-17 shows the input 1dB compression point for the LNA, measured when the signal generator sweeps the input power. It reaches –24dBm for high-gain mode.

Figure 4-18 shows the input 1dB compression point for low-gain mode, which is –30dBm. This is just slightly lower than the specified value and will not seriously affect receiver performance.

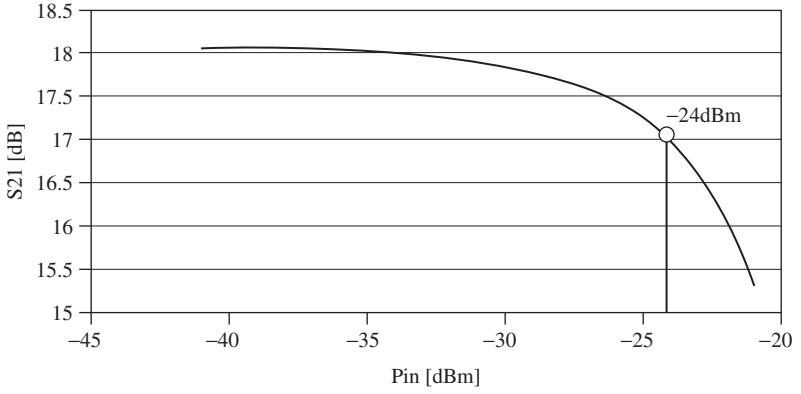


Figure 4-17 LNA high-gain mode 1dB compression point

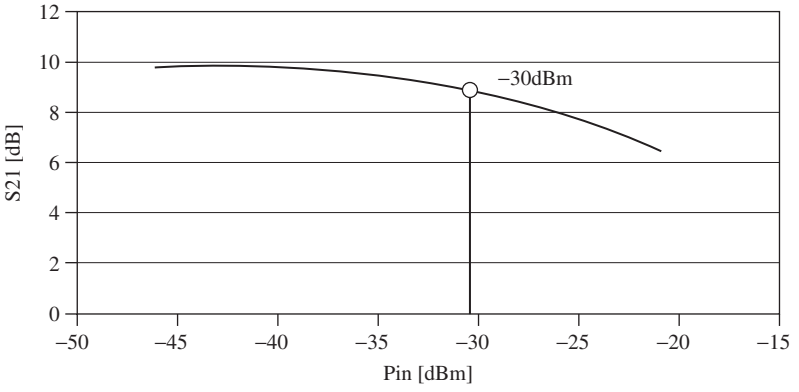


Figure 4-18 LNA low-gain mode 1dB compression point

Table 4-1 summarises the specifications and the results of the post-layout simulation and measurement. It can be seen that the input and output return loss measurements differ from the post-layout simulation results. This is due to the matching network and the paths of the PCB. However, it meets high-mode gain specifications. The gain is around 1dB less and the noise figure is 0.4dB higher than the typical mean post-layout simulation results for high-mode gain, as could be expected from the experimental results. However, as explained in the previous chapter, this is not a drawback. For low-gain mode, the gain and the noise figure meet specifications. The current consumption is slightly higher than specified. These are satisfactory results when considering the problems of amplifier stability that have arisen in the design stage.

The performance of the LNA, as shown in Table 4-1: can be compared to that of the LNA of state-of-the-art GPS front-ends shown in Chapter 1. Moreover, it must be remembered that the designed LNA includes ESD protections and has been measured in a package. Therefore, the results encompass the parasitic elements of these factors. Moreover, additional features are entailed, such as double-gain mode and the antenna detection sensor.

TABLE 4-1 LNA results

	Specifications		Post-layout		Measurement		
Parameter	**Gmin**	**Gmax**	**Gmin**	**Gmax**	**Gmin**	**Gmax**	**Unit**
S11	< –10		–14	–18.2	–7.5	–16.9	dB
S22	< –10		–7.6	–21.8	–8.3	–11.4	dB
Gain	8	20	10	19.7	9.5	18.5	dB
NF	10	2.5	3.5	2.8	5	3.2	dB
Current	<7		7.5		8		mA

4.4.2 RF Amplifier and Mixer Measurement

The RF amplifier and mixer have also been measured on the PCB. In the front-end chip, the measurement has been possible thanks to the intermediate pads located in the input of the mixer's LO. The input and output are available because they are connected to the external SAW and IF filter, respectively. This can be seen in the mixer area of the Figure 4-4.

The packaged RF amplifier and mixer have been measured using the test setups described in Figures 4-19 through 4-22.

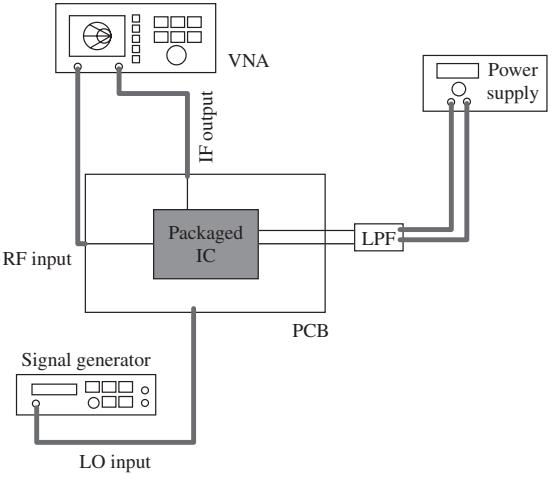


Figure 4-19 Test setup for measuring the S11 of the RF amplifier and mixer

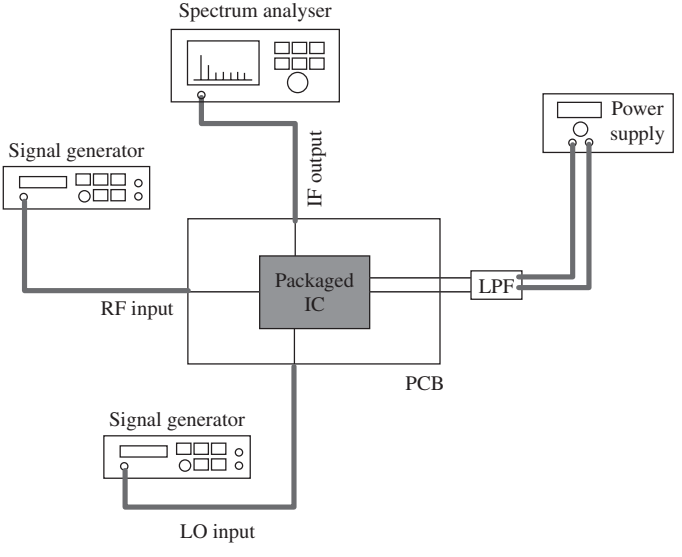


Figure 4-20 Test setup for measuring the conversion gain of the RF amplifier and mixer

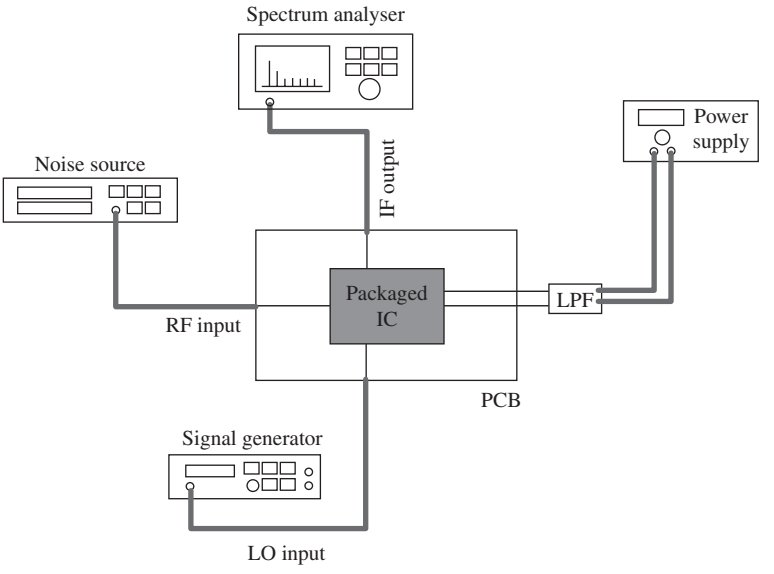


Figure 4-21 Test setup for measuring the noise figure of the RF amplifier and mixer

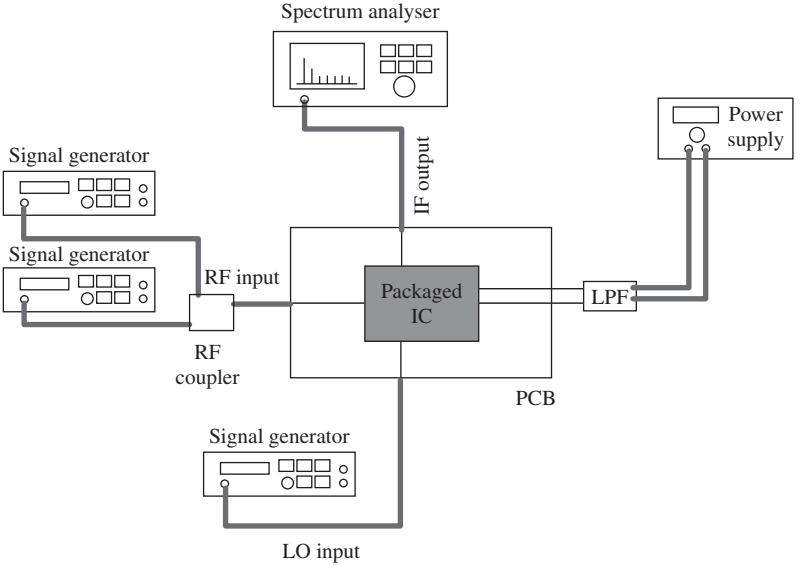


Figure 4-22 Test setup for measuring the IIP3 of the RF amplifier and mixer

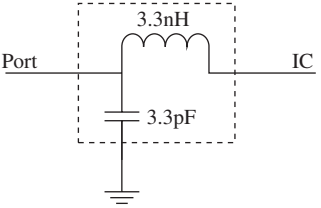


Figure 4-23 External matching network of the RF amplifier and mixer

Figure 4-23 shows the external matching network employed at the input of the RF amplifier and mixer.

Figure 4-24 presents the input return loss measured with a network analyser (Agilent E5071A), which is below –20dB at the working frequency.

Figure 4-25 presents the gain and the noise figure measured with the spectrum analyser (Agilent E4402B). The gain is 12.9dB and the NF is 6dB for a LO input power of 3dBm.

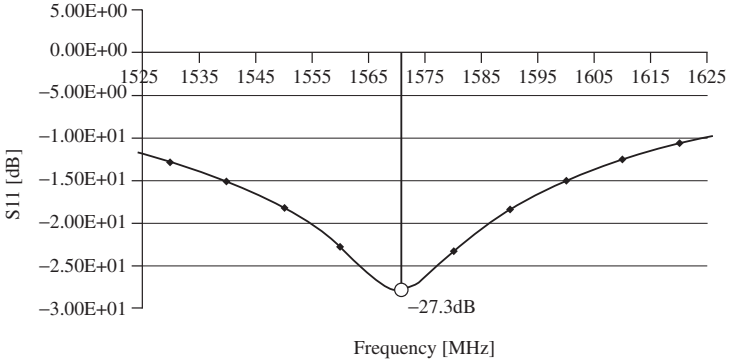


Figure 4-24 RF amplifier and mixer input return loss

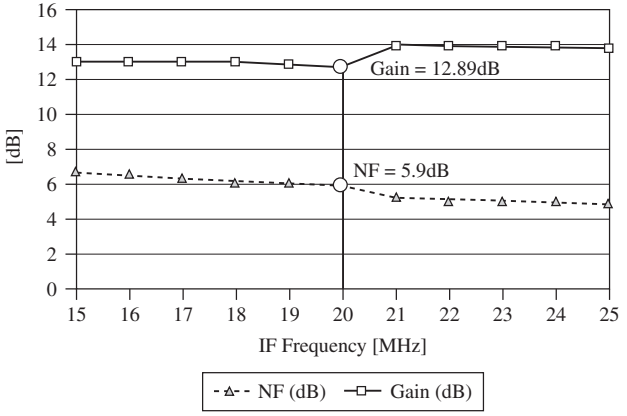


Figure 4-25 Gain and noise figure of the RF amplifier and mixer

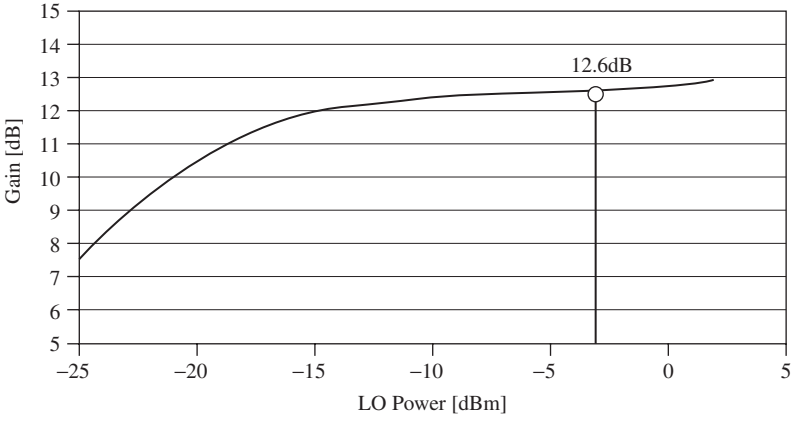


Figure 4-26 RF amplifier and mixer gain depending on LO input power

The influence of the LO input power on the conversion gain has also been measured. The conversion gain decreases 0.5dB when the LO input power varies from 3dBm to –8dBm. This variation is represented in Figure 4-26. Therefore, if the power at the PLL were lower than specified, but higher than -8dBm, the performance of the mixer would remain almost constant gainwise.

The measured third-order intermodulation point (IIP3) of –19dBm is shown in Figure 4-27. It has been measured with a two-tone input signal from two signal generators (Agilent E4421B) and the spectrum analyser (Agilent E4402B).

Table 4-2 summarises the results for the RF amplifier and mixer. With the exception of gain and linearity, all the parameters meet specifications.

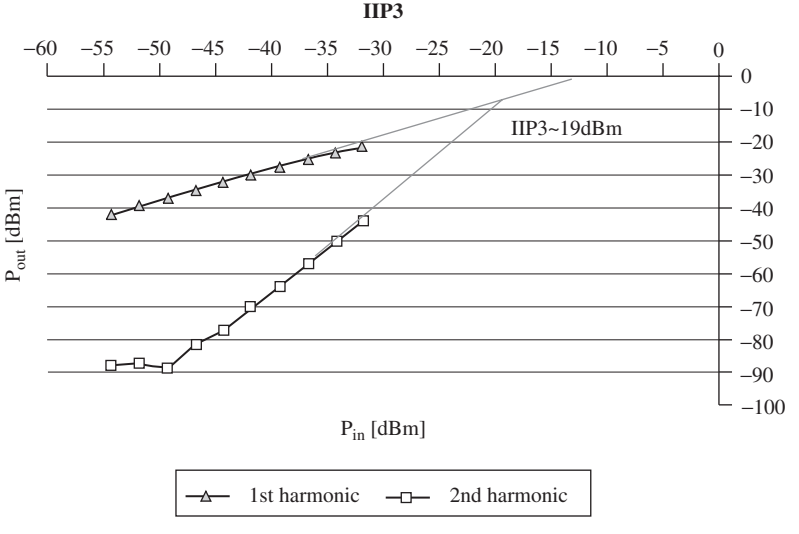


Figure 4-27 IIP3 of the RF amplifier and mixer

TABLE 4-2 Comparison between the parameters specified for the RF amplifier and mixer and the values estimated and measured in simulation

Parameter	Specifications	Post-layout	Measurement	Unit
Gp	23	18.1	12.9	dB
NF	6.2	5.6	5.4	dB
OIP3	1.5	0.5	–6.1	dBm
IIP3	–21.5	–17.6	–19	dBm
S11	<–10	–30	–27.3	dB
Current	<13	5.9	4	mA

Nevertheless, gain specification will not be a drawback as system gain will be compensated by a higher gain in the IF amplifier stage.

The slight decrease in linearity will lead to slightly worse performance against to possible interferences. The low level of power consumption is apparent, which is less than three times the value initially specified. Therefore, these results are suitable for the RF front-end. Comparing these results with a state-of-the-art device, it is worthwhile to mention that the RF amplifier and mixer, the measurement of which includes package and ESD protection, presents one of the lowest noise figures and relatively high gain.

4.4.3 IF Amplifier Measurement

The measurement of the IF amplifier has also been carried out on a PCB with an encapsulated IC. The connections of the IF amplifier have been made with the pins of the package specially made for the IF filter and the intermediate pads located next to the ADC.

Figure 4-28 shows the microphotograph of the IF amplifier. The figure shows the components of the IF amplifier: resistors, transistors, metal connections, and pads.

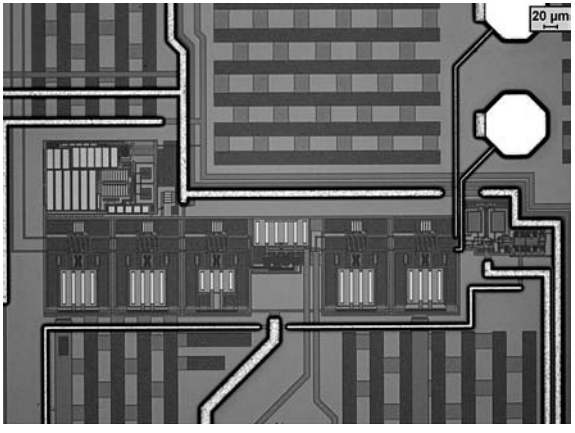


Figure 4-28 Microphotograph of the IF amplifier

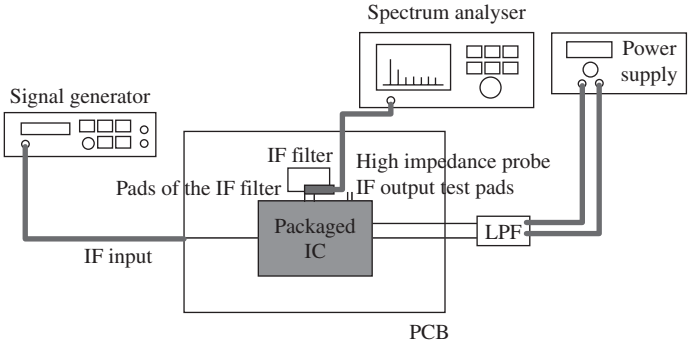


Figure 4-29 Test setup for measuring the gain of the first stage of the IF amplifier

The test setups required for measuring the performance of the IF amplifier are illustrated in Figures 4-29 and 4-30.

The gain and the power consumption of the amplifier can be measured with a sinusoidal input from a signal generator (Agilent E4421B) and a spectrum analyser (Agilent E4402B) with a high-frequency probe (Agilent 85024A), which presents an extremely low input capacitance of only 0.7pF shunted by 1MΩ of resistance. Therefore, the standard 50Ω of the spectrum analyser is avoided. Moreover, the probe allows direct measurement from the PCB. Consequently, no additional connectors are required on the PCB.

However, the insertion of the probe alters the load of the amplifier, thereby modifying its gain. To compare the experimental results with the values obtained from simulation, desginers should include the load added by the probe in the simulation environment. In this manner, the deviation from simulation results can be estimated for the amplifier's real load during normal operation.

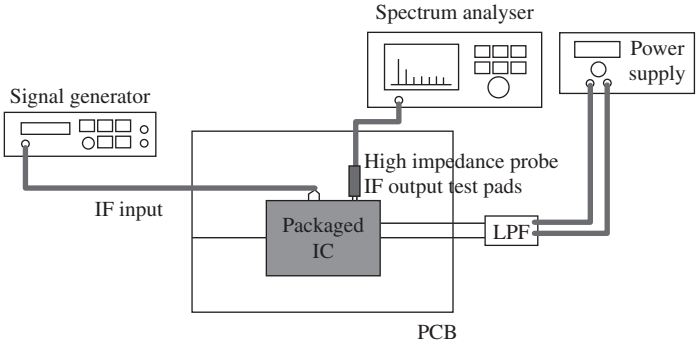


Figure 4-30 Test setup for measuring the gain of the second stage of the IF amplifier

TABLE 4-3 IF amplifier results

	Specifications	Post-layout	Measurement	Unit
G	>42	68	67 (47+20)	dB
Current	3	2.4	2.5	mA

The total gain of the IF amplifier is 67dB. This value is obtained in two stages: A gain of 47dB is introduced in the first IF amplifier stage and 20dB in the second IF amplifier stage. Both amplifiers have been measured separately. This is mainly due to the fact that the second stage of the IF amplifier lacks an output buffer and is therefore unable to amplify properly with the load modification introduced by the pads, bondwires, package leads, and the high-impedance probe.

Table 4-3 summarises the specifications and the post-layout and measurement results. It can be observed that the gain and the current specifications have been met.

4.4.4 ADC Measurement

The measurement of the ADC, either directly or separated from the rest of the RF front-end, is not possible through the use of any of the bonding configurations utilised for measurement.

The ADC is a simple 1bit converter that consists of just one D flip-flop. Its simulation was obtained from the 200-sample Montecarlo analysis and is expected to have a stable experimental performance.

Furthermore, the samples required for measuring the offset level of the ADC are unfeasible for the standard design process of an RF front-end (a MPW for the case of the design example of this book). On the other hand, the correct performance of the ADC can be tested together with the entire front-end. A microphotograph of the ADC is shown in Figure 4-31.

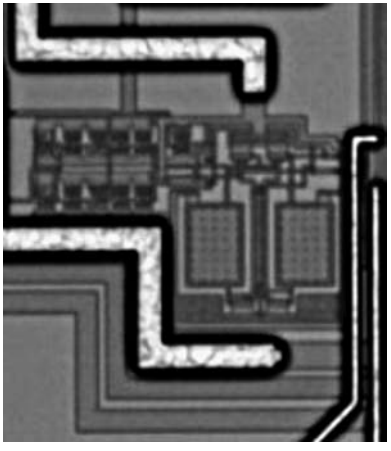


Figure 4-31 Microphotograph of the ADC

4.4.5 Control Logic Measurement

As explained in the previous chapter, different operation modes can be set by means of integrated logic. A microphotograph of integrated logic components is shown in Figure 4-32.

The performance of the control logic can be measured through the current consumption of the integrated circuit. Consequently, the current variation through the different operational states of the RF front-end can be measured.

The current consumption for the designed and fabricated IC is 23mA when the entire RF front-end is switched on. When in stand-by mode, the current consumption decreases to 0.5mA. When only the digital parts are on, the current consumption is 1.5mA in order to provide the clock signal. Finally, in the case of the test mode, the current consumption changes depending on the voltage applied to the Frequency Selection (FS) pin.

4.4.6 PLL Characterisation

The PLL plays a major role in the design of a dual RF front-end for a dual GPS and Galileo receiver with low-IF architecture, such as the one explained in this book. The PLL is responsible for the frequency translation of the received signal. Among other undesired effects, it contributes, along with the phase noise, to the increase of the effective noise figure of the complete front-end and reduces its blocking performance. Therefore, before the characterisation of the complete RF front-end is attempted, it is mandatory to characterise the PLL separately.

To quantify the performance of the PLL integrated with the rest of the IC, intermediate pads located at the inputs and outputs of the PLL blocks are required. This enables the characterisation of both the PLL and its blocks.

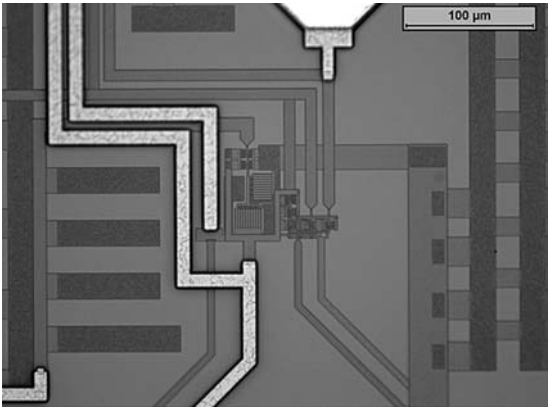


Figure 4-32 Microphotograph of the control logic measurement.

The upper-left part of the microphotograph in Figure 4-4 shows the PLL, in which the intermediate pads can be easily identified. To measure output power, oscillation frequency, and current consumption, a test setup such as the one described in Figure 4-33 is required. In the case of the fabricated RF front-end, the results are described in the following paragraphs.

The current consumption of the PLL is around 8.7mA, from which the prescaler consumes approximately 2mA, the pierce oscillator less than 500μm, and the VCO 6.3mA.

The output power of the PLL is between –11dBm and –12.5dBm for the tuning range between 0.5V and 2.8V. The characteristics of the measurement test setup suggest that the actual performance of the PLL could be slightly better than the measured one. The measurement test setup uses a spectrum analyser, which presents a 50Ω input impedance. The buffer of the VCO is usually designed to drive the mixer LO input and the divider of the PLL. Therefore, the load of the buffer presents higher impedance during normal operation. The buffer is an emitter follower stage. This configuration does not add any gain to the system but isolates the tank of the VCO from the output load. During this stage, a high-impedance tank is usually achieved, as is, consequently, large output power with reasonably low current consumption. An impedance of 50Ω on the other side of the buffer slightly reduces the impedance of the resonance tank. This results in the reduction of the voltage swing of the signal by decreasing not only the output power but also by increasing the phase noise.

Regarding the characterisation of phase noise, using a set of batteries to provide the power supply is highly recommended. This minimises the possible noise introduced by the power supply system. The connection between the set of batteries and the PCB should be made with the shortest pair of twisted cables available, in the quietest electromagnetic environment possible.

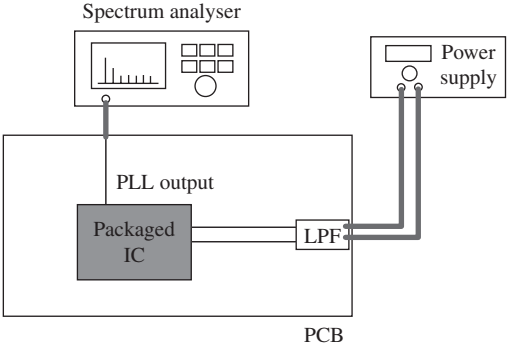


Figure 4-33 Test setup for the characterisation of the current consumption, oscillation frequency, and output power of the PLL

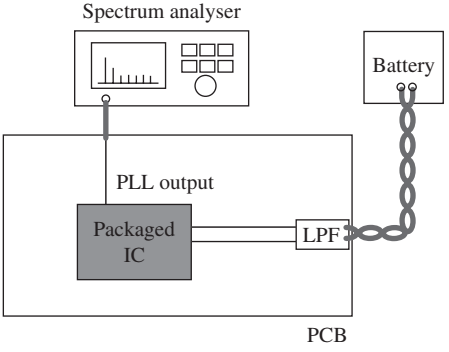


Figure 4-34 Test setup for the characterisation of the phase noise of the PLL

Figure 4-34 illustrates the test setup utilised for the characterisation of the PLL phase noise.

The phase noise characteristic of the fabricated PLL is illustrated in Figure 4-35. The VCO, the divider, the PFD, the charge pump, and the loop filter are the main contributors to the total noise. The measured values show that at 100kHz from the fundamental tone, the phase noise is around –84dBc, which could be expected from the simulation results. Although the measured value is slightly higher than the specified one, such difference does not affect the performance of the receiver. This is explained in detail in the PLL design section (section 3.6) of the previous chapter.

It is worth mentioning that although short, twisted cables are used with a set of batteries, spurious tones tend to be captured by the PLL feeding system. These spurious tones are translated to the side bands of the PLL output and distort the measured phase noise values. It is important to distinguish these tones because, as they are not introduced

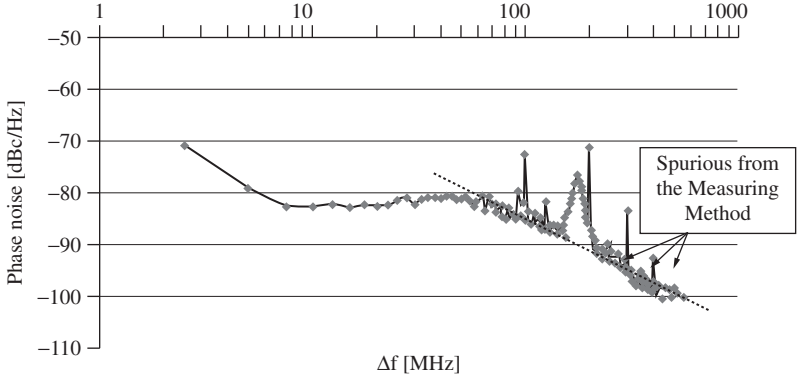


Figure 4-35 Phase noise response of the PLL

by the PLL, they should be discarded. These tones are usually caused by lightning systems, PCs, or other electronic equipment operating in the vicinity.

Table 4-4 summarises the specified values, the post-layout simulation results, and the measured characteristics. The value of the output power in the table corresponds to the value measured with the 50Ω load of the spectrum analyser. The output buffer of the VCO has been designed to drive loads of the mixer and the divider of the PLL. Therefore, for a lower load, a lower value of the output power is obtained. However, the 50Ω load of the measurement equipment and the additional bonding wires can be considered and included in the simulation environment. This results in the matching of the output power obtained from the simulation to the measured value. Therefore, it could be stated that the actual output voltage driving the mixer is within the specified range of 0dBm to 3dBm. On the other hand, if the output power were slightly lower than the value specified due to the characteristics of the mixer, the final performance of the receiver chain would hardly vary.

Though the measured frequency of the PLL range meets specifications, it is higher than that predicted by the simulations. This is due to the overestimation of the parasitic capacitances of the metal paths of the VCO. The safety margin introduced in the locking range of the PLL ensures the correct oscillation frequency of the PLL.

The second-order harmonic and the current consumption results are just slightly higher than the value specified and are therefore acceptable.

4.4.6.1 VCO Measurement The variation of the oscillation frequency with the tuning voltage of the VCO can be measured with the same bonding configuration of the PLL but without connecting the PLL filter to the tuning voltage pin of the VCO.

Figure 4-36 illustrates the test setup required for measuring the variation of the oscillation frequency with the tuning voltage.

TABLE 4-4 Specified characteristics of the PLL, values estimated from post-layout simulations and measured values

Parameter	Specification	Post-layout [2.8V/0.5V]	Measurement [2.8V/0.5V] *with a 50Ω Load	Unit
Output power	0–3	1.26/2.69	–11/–12.5	dBm
Frequency	1.544 & 1.571	1.513/1.729	1.509/1.750	GHz
Phase noise	–90 at 100kHz	–97/-81	–84	dBc/Hz
Second-order harmonic	–23	–39/–37	–22.6	dBc
Current Consumption	<9	10	10	mA

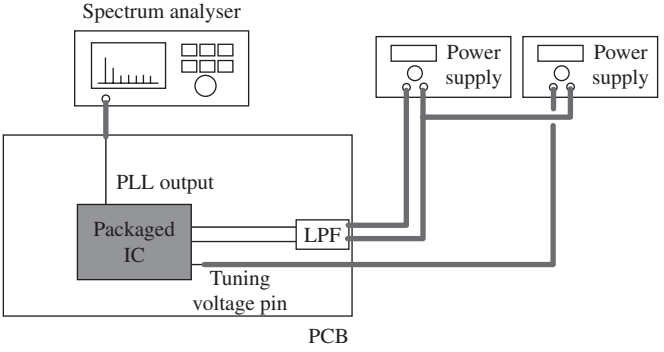


Figure 4-36 Test setup for measuring the oscillation frequency of the VCO for different tuning voltages

The output frequency is 1.750GHz for a control voltage of 0.5V and 1.509GHz for a control voltage of 2.8V. Both the working frequencies, 1554.960MHz and 1571.328MHz, lie within this range. The variation of the oscillation frequency with the tuning voltage is shown in Figure 4-37.

The gain constant (*Kv*) of the VCO is shown in Figure 4-38. The measured values presented in the figure demonstrate that both working frequencies are within the range of the VCO, proving that the VCO works properly for this application. The current consumption of the VCO is 6.3mA where the core itself requires 3mA.

4.4.6.2 Pulse Swallow Divider Measurement One of the blocks that is worth measuring is the pulse swallow divider. Most of the uncertainties related with the possible malfunction of a PLL disappear when characterising this block of the PLL. The measurement of this block provides a key

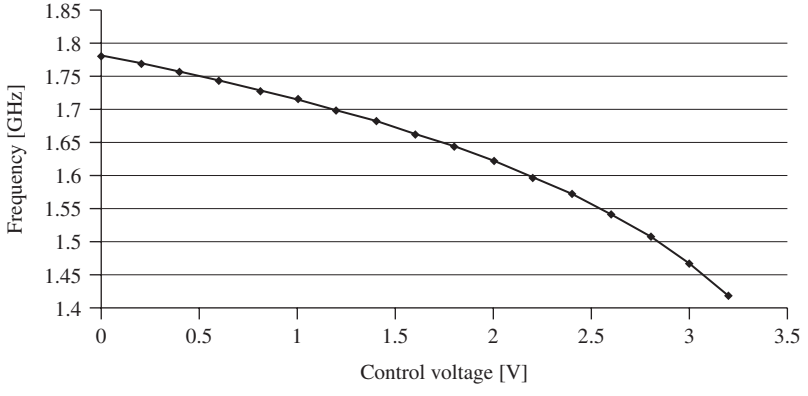


Figure 4-37 VCO output frequency depending on control voltage

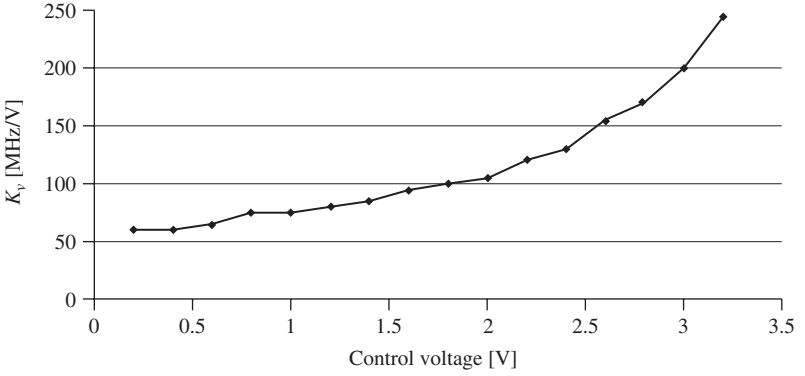


Figure 4-38 Variation of the gain constant of the VCO with the control voltage

insight into the performance of the local oscillator of the RF front-end. The test setup required for measuring the pulse swallow divider is illustrated in Figure 4-39.

In the fabricated RF front-end, the entire pulse swallow divider can be characterised as a whole. The sub-blocks that compose the pulse swallow divider (such as the prescaler, the program counter, and the swallow counter) cannot be separately measured in this design example.

The pulse swallow divider has to divide the signal frequency by 95 or 96, depending on the state of the control pin. Working frequencies have provided satisfactory results for the fabricated chip.

Special attention must be paid to filtering the noise coming from the power supply, which can cause the divider to malfunction, especially at higher frequencies. Higher robustness to power supply noise can be reached by minimising the parasitic capacitances of the circuit.

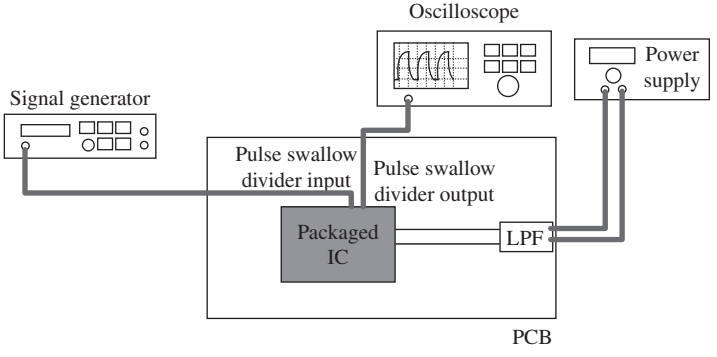


Figure 4-39 Test setup for measuring the performance of the pulse swallow divider

In addition, as explained in the circuit design, basic gates of the foundry library should be, in certain situations, modified to minimise their parasitic capacitance. This capacitance may create a delay in the signal that could make the divider slower than required. Moreover, parasitic capacitances of the prescaler's D flip-flops also make switching time longer and thus not suitable for higher frequencies.

4.4.6.3 Phase Frequency Detector and Charge Pump Measurement To reduce uncertainties, the static and dynamic behaviour of the PFD and charge pump should also be measured. These can be measured because their input and output are accessible and do not required any extra special pads (other than those already employed) nor a special bonding configuration. The inputs can be set externally from the crystal pad for the first input of the PFD (PFD1) and the divider input pads (output of the VCO) for the second one (PFD2).

Table 4-5 shows the static behaviour of the PFD and the charge pump. It can be seen how the upper and the lower transistors of the charge pump are switched depending on the input, dictating whether the load capacitor is charged or discharged. When both inputs are high, charge pump transistors are "on," leaving the charging and discharging paths open at the same time. This is why the output is a nondefined state that remains at 1.4V.

Dynamic behaviour can be measured by connecting a capacitor of 150pF to the charge pump. The output is high when PFD1 is high and PFD2 is low. If PFD1 changes to low, output also tends to be low. The simulated and measured results are shown in Figure 4-40. The measured results confirm the predicted behaviour.

4.4.6.4 Crystal Oscillator Measurement The performance of the crystal oscillator can be measured on the PCB connected to a quartz crystal and its associated capacitors. The current consumption is around 1mA. The output has been taken from an IC clock pin. Figure 4-41 shows the 16.386MHz frequency clock signal in the spectrum analyser. Figure 4-42 shows the test bench and clock signal on the oscilloscope.

TABLE 4-5 Static behaviour of the PFD and charge pump

PFD1	PFD2	Output
Low	Low	Low
Low	High	Low
High	Low	High
High	High	1.4V

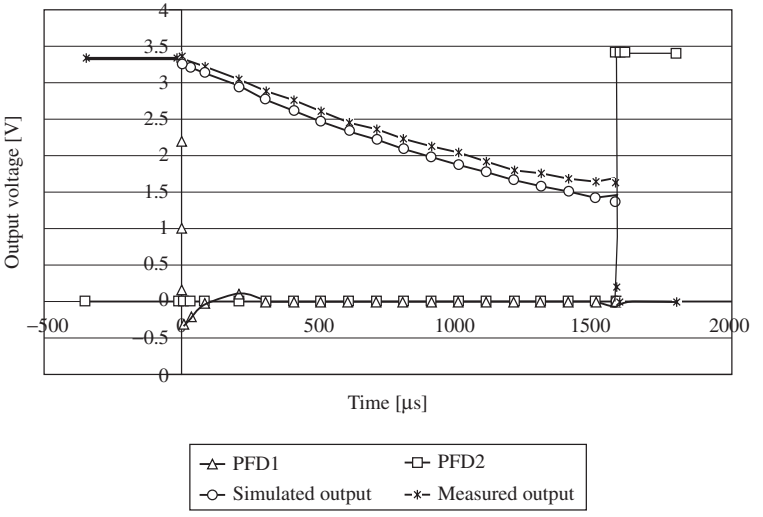


Figure 4-40 Dynamic behaviour of the PFD and charge pump

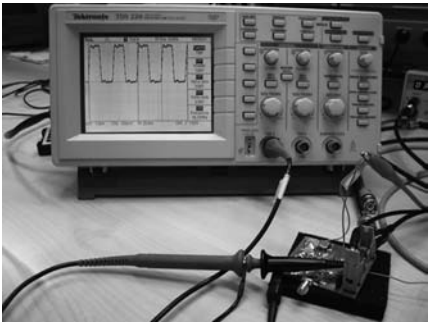


Figure 4-41 Spectrum of the clock signal

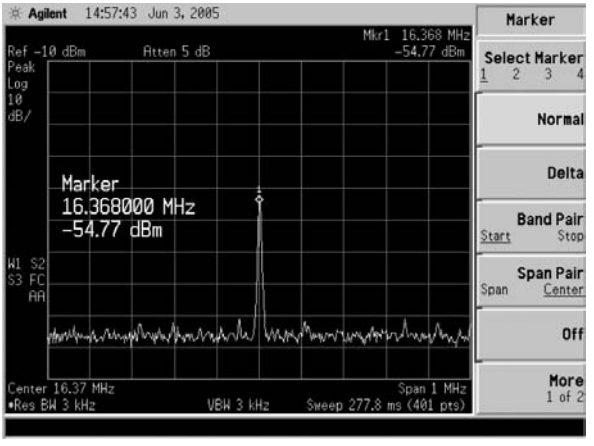


Figure 4-42 Clock signal in the oscilloscope

4.5 Characterisation of the Complete RF Front-End

The complete RF front-end requires a bonding configuration, illustrated in Figure 4-43, different from the one employed for the characterisation of the blocks.

The packaged IC also requires a PCB assembled with discrete components needed for correct operation, such as decoupling capacitors, a SAW filter, LC filters, a crystal oscillator, and connectors.

Figure 4-44 shows the circuit schematic of the previously mentioned PCB and details the components used for the characterisation of the fabricated PCB.

The test setup that can be used to characterise the complete RF front-end is illustrated in Figure 4-45.

The overall performance of the front-end in terms of power consumption, gain, and noise figure has been obtained for a supply voltage of 3.3V and an RF input signal of 1.575GHz. These features are summarised in Table 4-6.

The output signal of the designed front-end has been compared to a commercial front-end. The comparison has been made with a single sinusoidal input signal of the following characteristics: 1575.42MHz and 122dBm.

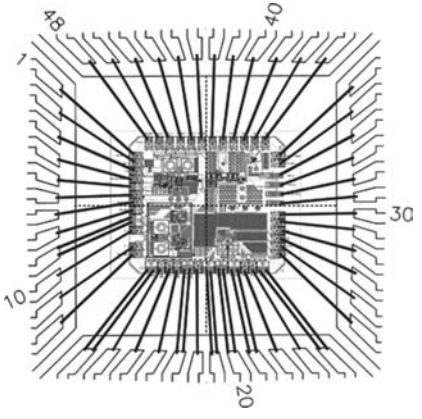


Figure 4-43 Bonding diagram for the final application

TABLE 4-6 Receiver measured results

Process	0.35µm SiGe
Current consumption	23mA
Front-end bandwidth	6MHz
Voltage gain	103dB
Noise figure	3.7dB
Front-end size	2.8x3.0mm^2

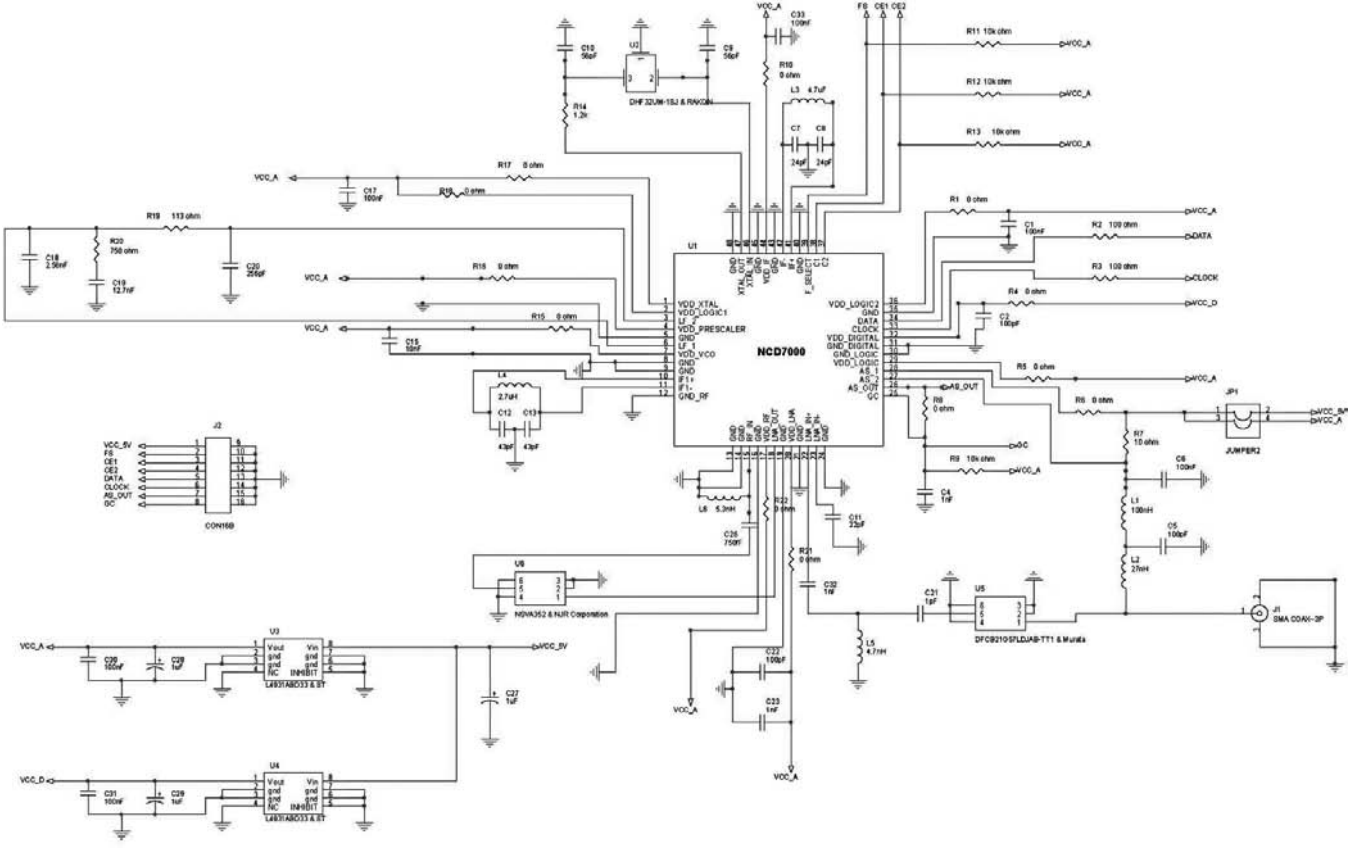


Figure 4-44 Circuit schematic of the PCB required for the characterisation of the RF front-end

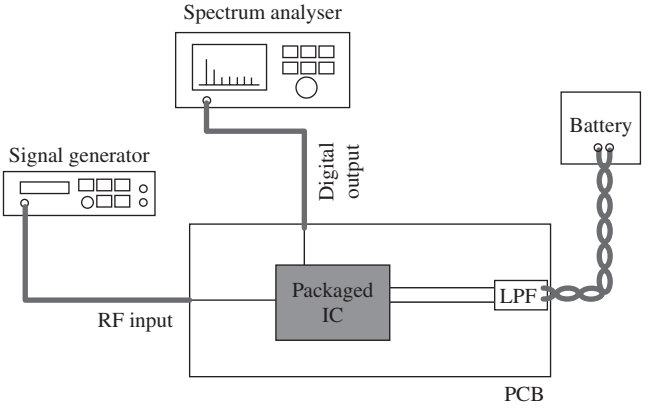


Figure 4-45 Test setup required for the characterisation of the RF front-end

Figure 4-46 shows the spectrum of both output signals. Four tones can be clearly identified: The first one, at 4.092MHz, corresponds to the navigation data frequency and the other three tones are the sampling frequency tone at 16.386MHz, while the other two sampling tones are at 16.386±4.092MHz. The output signal shows that the designed front-end presents a slightly higher gain than the commercial one. The noise level is lower, which improves the output signal-to-noise ratio (SNR). Due to these characteristics, the designed receiver is expected to have

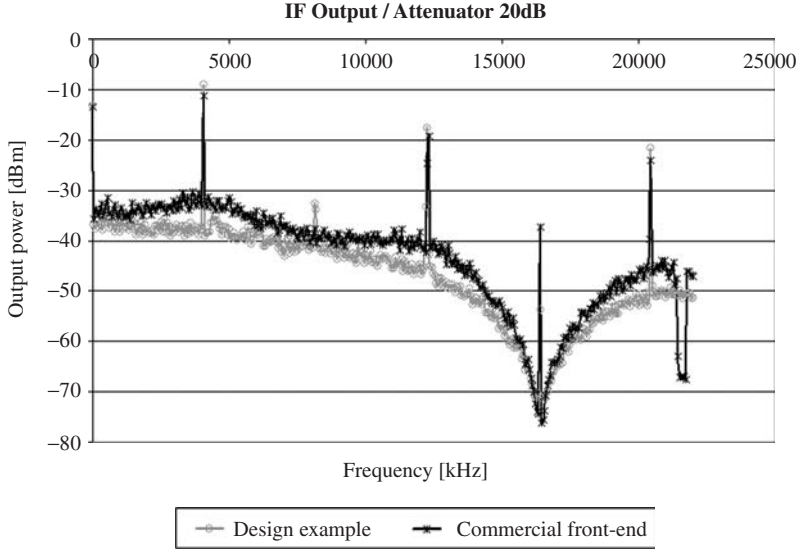


Figure 4-46 Output signal of the designed front-end and a commercial front-end

higher sensitivity. Thus, it is suited for positioning in adverse environments such as urban areas or forests.

4.6 Summary

In this chapter, the designed GPS and Galileo RF front-end has been fabricated and measured. First, the stages in the validation of an integrated circuit were shown. Then, a method for the validation of the different blocks inside the front-end and the entire front-end IC was set. Experimental results of the blocks have been obtained by means of different test setups, which are presented in this chapter. As was expected, the obtained results have been slightly worse than the post-layout results. However, this is no drawback for the operation of the receiver. The front-end can be included in a GPS/Galileo receiver to obtain the position more accurately through their interoperability. Finally, the front-end has been compared to a commercial one, obtaining a better performance.

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Chapter

5

Applications

A number of fields will benefit from a dual GPS/Galileo receiver combined with other technologies. This chapter briefly introduces some of the fields and aspects that will be positively impacted by this device. Once the RF front-end has been verified, a system should be developed to check whether the designed RF front-end works for a specific application. To gauge the performance of the front-end within a receiver, a full-solution platform is required. Therefore, to integrate the design example of this book, the development of a navigation module for the automotive industry is given as an example. This not only allows for the verification of the receiver in a static case by mimicking the conditions of lab measurements, but also for that of the front-end in a high-speed and dynamic environment.

A complete Global Navigation Satellite System (GNSS) receiver is composed of the analogue element (antenna and RF front-end), digital signal processing, which obtains the information coming from the receivers; and map-managing and user interface hardware and software. Apart from the selected antenna and the RF front-end developed in this book, a commercial processor has been selected to set the coordinates using navigational data. Then, an on-board PC and a LCD screen suitable for car use for the receiver has been chosen and a software has been developed to acquire navigational data and manage maps.

5.1 Fields of Application

GPS/Galileo-based applications can be found on land, on water, and in the air. The system can be employed wherever satellite signals can reach the end user's receiver. This, of course, is not the case where it is impossible to receive signals, such as inside buildings or within subterranean or submarine locations, among other locations.

The most common air applications are for navigation by general aviation and commercial aircraft. It is also typically used for navigation by recreational boaters, commercial fishermen, and professional mariners. The scientific community also employs precision timing capability and position information. Surveyors save money by drastically reducing setup time at the survey site and providing highly accurate measurements. Recreational uses, which are as numerous as recreational activities themselves, will benefit from improvements in satellite navigation where location, position tracking, or direction plays an important role.

Several applications that can take advantage of the GPS/Galileo receiver together with the use of other technologies are listed as follows [EU-Galileo]:

- **Road** The road sector is a major potential market for satellite navigation-based applications, since they are already commonly installed in new cars as a key tool for providing new services to people on the move. These include electronic charging, real-time traffic information, emergency calls, route guidance, fleet management, and Advanced Driving Assistance Systems (ADAS). Apart from these features, drivers, car manufacturers, and law enforcement officials can benefit from the increased availability of satellite navigation services in advanced car navigation systems. They can also reap the rewards of reduced travel time, demand management, and traffic monitoring and increased confidence in fleet management and tracking of goods in all industry sectors.
- **Rail** A number of rail transport applications—ranging from traffic, wagon, and cargo control and monitoring to train signalling, track survey, and passenger information services—will be offered, making it possible to reduce distances between trains and therefore increase train frequency. In addition, such applications will make it easier to locate the entire rail fleet. These applications will increase rail transport performance and facilitate a massive transport shift from road to rail, reduce trackside equipment, and provide additional economic benefits for train control. Furthermore, the benefits of high positioning accuracy for efficient track surveying, a unique tool that contributes to a number of different functions, are bound to be significant.
- **Aviation** Satellite navigation has already been used as an additional means of localisation, which helps many aspects of aviation in both commercial and noncommercial air transport alike. Ground movement, taking off, en-route flying, and landing in all weather conditions will reach the required level of safety necessary to cope with the continuous increase in flights. Air traffic management will be optimised for rapidly growing air traffic, and airport infrastructures will be able to guarantee better traffic control and safety, which will be

increased by means of system redundancy between GPS and Galileo. The benefits offered to the aviation community will include the following: increased safety through an additional independent satellite constellation with no common modes of failure, a navigation system built to aeronautical safety requirements, high system performance to complement ground infrastructure, increased safety of navigation in all flight phases, increased efficiency in flight operations management, improved airspace utilisation, and safer navigation of rescue helicopters under all weather conditions.

- **Public transport** Traffic congestion, pollution, and other negative aspects will be reduced with the optimisation of public transport. The public transport sector can benefit from improved services and lower costs, efficient fleet usage with better coverage of different urban zones, increased driver security, new solutions for car pooling, and improved car navigation systems.
- **Maritime** Innovation and progress will be brought to navigation and activities such as fishing, oceanography, and oil and gas exploitation in order to increase the efficiency, safety, and optimisation of marine transportation. All marine applications, including recreational boats, commercial vessels, and unregulated and safety of life at sea (SOLAS)–regulated ships will benefit from a reliable, safe, and accurate tool for maritime navigation in any phase. In addition, integrity information for Safety-of-Life and improved search and rescue (SAR) services will see significant benefits.
- **Safety** Risks for travellers and working crews will be reduced and lives will be saved through increased route guidance capabilities and advanced driver assistance systems. Other benefits include better air traffic management, more reliable positioning information for trains and boats, better fleet management and en-route guidance of emergency services, effective tracking of dangerous or valuable goods during their transportation, and more effective monitoring of infrastructures.
- **Energy** Improvement will also be seen when it comes to the control of energy infrastructures. These benefits include improved power flow, enhanced time-synchronisation of power-related instruments, increased safety and efficiency in oil exploration, improved control of drilling facilities, and faster positioning information, even in remote areas.
- **Telecommunications** A synergy between satellite-navigation applications and telecommunications will increase the level of communications and the efficiency of their networks. For example, receivers with mobile phones will generate a multitude of combined uses for the making of emergency calls (E-112 in Europe, E-911 in the United States) or for new services based on location, direction, or real-time

traffic information, among others. This will provide a precise and low-cost tool for network synchronisation, ensure the stability of synchronisation, increase communication traffic via Location Based Services (LBS), offer customised services to clients, and increase pricing and billing flexibility.

- **Finance, banking, and insurance** The digital lifestyle that so many of us lead requires the transmission of sensitive data every day. Therefore, security, data integrity, authenticity, and confidentiality have emerged as major issues in the electronic exchange of documents. The protection of such information is vital, and the latest encryption and authentication techniques are ever-evolving. The following will be offered: a common, validated time reference at low cost; availability of advanced and simple security modules for low-cost encryption; simple and secure transactions with easily authenticated electronic documents and data; a secure tool for e-commerce applications; satisfied insurance companies and users; and fewer risks in highly sensitive operations.
- **Civil engineering** This field, which relies on accuracy and reliability, will benefit from decreasing costs and increasing efficiency. Combined with digital mapping, a powerful tool for improving productivity will be offered, spanning the planning of structures to the maintenance and surveillance of existing construction projects. Together with other technologies, GPS/Galileo technology will make it possible to improve logistics and optimise human resources, which will lead to increased efficiency with no loss in quality and increased safety on the construction site.
- **Agriculture** Food security issues will be managed in a more efficient way to overcome consumer concerns. The quality of agriculture will improve while respecting the environment. Together with other technologies, GPS/Galileo technology will help minimise the distribution and dilution of chemicals, improve parcel yield from customised treatment, and lead to more efficient property management.
- **Fisheries** The needs of the fishing sector range from day-to-day operational support to the navigation and positioning of fishing vessels. Strict international rules governing intrusion into national waters demand that vessels are monitored to ensure that they fish only within designated areas. It will be possible to obtain a more effective exchange of information between vessels and stations, improve fishing capabilities, and enhance navigational aids for fishermen.
- **People with disabilities** A key benefit of these kinds of applications and services is to provide technological assistance for people with disabilities in a variety of situations, by increasing the availability

of support services, especially in inner-city areas. Some application examples may include personal navigation assistance for people with impaired vision; assistance for Alzheimer's patients with memory loss; route planning for people with physical disabilities; enhancement of telemedicine or emergency services through real-time localisation; and real-time public transport audio announcements regarding remaining travel time, stops, and connections.

- **Civil protection** Disaster management will reap significant benefits as additional lives will be saved thanks to a space-based system with global coverage and round-the-clock availability, reliable positioning, and optimisation of rescue operations and resources. These will be available in difficult environments and even when local infrastructures and services may be temporarily unavailable.
- **Time reference** Not only is the high accuracy time disseminated by the modern GPS and Galileo advantageous, but so is the technology's interoperability with applications that require a common time reference. Examples include wireless telecommunication network management or power plant and network monitoring. Moreover, applications that require certified time stamps will also benefit, such as electronic banking, e-commerce, the stock exchange, and quality assurance systems and services. Other applications may include traffic light regulation, certified documentation production, and so on.
- **Science** An improvement to data collection in the area of environment monitoring will aid in the analysis of polluted areas; studies of tides, currents, and sea levels; tracking of icebergs; and the study of tectonic movements. An improved instrument capable of continuously tracking wild animals will be crucial in the study of biology and animal behaviour. A miniaturised receiver can be attached with a collar to monitored or protected animals to follow the movement and migration of species that might be in danger. This is important for the study of behaviour and for the monitoring and preservation of habitats.
- **Leisure** Apart its use in recreational flying or boating, a navigator for amateur users will provide personal information by means of handheld terminals combined with a map display and with secondary communication functions integrated with mobile communication technology. In this area, the key difference between the actual receivers and the ones allowing to integrate other communications technologies, is its focus on interoperability issues, which easily allow for integration (at the system and user level) with other existing and future systems (Global System for Mobile Communications [GSM], Universal Mobile Telecommunications System [UMTS], etc.).

5.2 Application Module for Cars

GPS/Galileo navigators will be commonplace in automobiles as well. Some basic GPS systems are already in use and offer emergency roadside assistance with just the push of a button, by transmitting the car's current position to a centre station. More advanced systems even show the car's position on a street map. Currently these kinds of systems allow any driver to know his or her position and even recommend the best route to reach the driver's destination. This section shows the development of such a navigation car module, which consists of a receiver module combined with the RF front-end design example described in this book and a navigation module.

5.2.1 Receiver

A GNSS receiver is able to pinpoint the position of the user from the signal sent by satellites. The navigation data are received by the antenna, down-converted by the RF front-end, digitalised in the analogue-to-digital converter (ADC), and correlated and processed by the processor in order to obtain the Position Velocity and Time (PVT).

Chapter 2 explained acquisition, down-conversion, and digitalisation. These are the main functions of the RF front-end. However, a processor is required to complete a receiver. The digital part of the receiver consists of a correlation digital signal processing (DSP), responsible for the demodulation of the signal, and a central processing unit (CPU) that processes the information sent by satellites.

The correlation consists of a demodulation of the signal with the respective satellite code. However, the received signal usually presents a delay in phase, as well as in frequency, compared to the original signal. Thus, the PR code has to be modified in phase and frequency to adapt it to the received signal.

Some devices are able to process 12 channels in parallel, managing all 12 respective PR codes in unison. In this case, receiver complexity increases, but performance is improved. Four satellites are enough to obtain the receiver's position, and redundant information is obtained to correct errors in accuracy. Moreover, when a satellite is out of view, the code for the next satellite in view can be calculated, decreasing the needed correlation time.

The demodulated signal is then processed in the CPU in order to obtain the receiver's position. Afterwards, the information is processed to be sent to the interface of the user. Therefore, a processor is required to combine a complete receiver with the front-end of this project. To make it suitable to the designed RF front-end and ensure optimised receiver performance, you must consider the following key criteria when selecting the processor:

- Highly integrated single solution: processor and correlation DSP in one chip
- High number of processed channels
- 3.3V voltage supply
- Low power consumption
- Small size
- Short time to first fix (TTFF)
- Clock frequency of 16.368MHz
- 1bit input signal

The GPS processor ST20GP6 [STGipsy], which fulfills the aforementioned requirements, has been selected. The data input is serial 1bit data, the clock frequency is 16.368MHz, and the power supply is 3.3V, making it suitable for the RF front-end. It integrates a 12-channel GPS correlation DSP, a CPU with microcontroller style peripherals, static random access memory (SRAM), read-only memory (ROM), and so on. The navigation data output is implemented through the serial port (RS232).

The receiver will be made up of the ST20GP6 [STGipsy] and the design example RF front-end of this book. The GPS signal will be received by the antenna, down-converted, and digitalised by the front-end. Then the digital element will process the signal to get the PVT information. The receiver diagram is shown in Figure 5-1.

5.2.2 GPS Processor

The ST20GP6 [STGipsy] is an application-specific single-chip micro using the ST20 CPU with microcontroller-style peripherals added on-chip. It incorporates DSP hardware for processing signals from GPS satellites. The 12-channel GPS correlation DSP hardware is designed to handle 12 satellites, two of which can be initialised to support the RTCA-SC159 specification for the Wide Area Augmentation Service (WAAS) and European Geostationary Navigation Overlay System (EGNOS) services.

Designed to minimise system costs and reduce the complexity of GPS systems, the ST20GP6 [STGipsy] offers all the required digital functions on one chip, including 64 KBytes of SRAM and 128KBytes of mask ROM. It supports large values of frequency offset, allowing the use of a low-cost oscillator while maintaining excellent TTFF performance. The CPU and software have access to the part-processed signal to enable accelerated acquisition time.

The ST20GP6 [STGipsy] can implement GPS digital signal processing algorithms using less than 50 percent of the available CPU

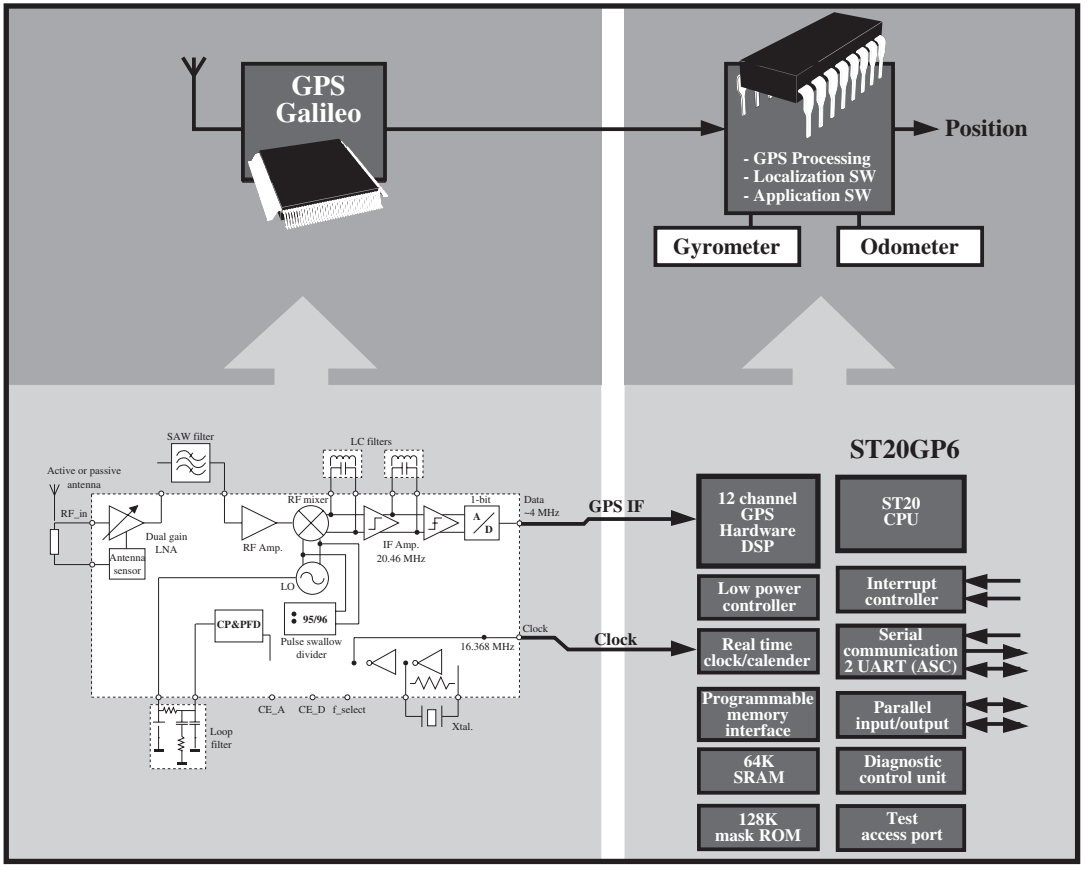

Figure 5-1 GPS receiver

processing power. This leaves the rest available for integrating original equipment manufacturer (OEM) application functions such as route finding, map display, and telemetry. Other characteristics are shown in this list.

- 32bit ST20 CPU
- 2-channel GPS correlation DSP
- 64Kbytes on-chip SRAM
- 128Kbytes mask ROM
- Programmable memory interface
- Serial communications
- Vectored interrupt subsystem
- Power management
- 3.3V, 0.35μm CMOS technology
- Diagnostic control unit
- JTAG test access port
- PQFP100 package

5.2.3 Navigator

The GPS receiver has been integrated into a system to provide a user-friendly interface. The navigator structure is a simple modular structure, as shown in Figure 5-2. It is basically composed of the GPS receiver, a PC, and a screen. The core of the architecture is an industrial PC, which allows the interconnection of all the basic elements of the system as well as other components that improve the features of the navigator.

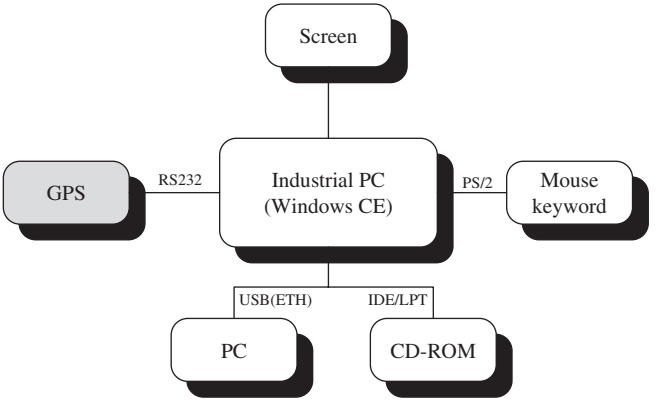

Figure 5-2 Navigation module block diagram

Navigation software has been developed enabling the PC to connect to the GPS, obtain information, and provide the user with coordinates on a graphical interface.

The navigator prototype is shown in Figure 5-3. The receiver, PC, and screen are integrated within a single module suitable for the dashboard of a car. The touchscreen protrudes slightly from the module, hiding the rest of the electronics. Moreover, as explained previously, other applications can be connected to the PC via USB and so on.

Satisfactory receiver performance has been noted for GPS. Nevertheless, the same navigator and method can be carried out to gauge how well Galileo performs. For this task, a Galileo processor is required. Currently no commercial Galileo processors are available on the market. However, in the future, manufacturers will offer GPS/Galileo processors suitable for the GPS/Galileo front-end covered in this book.

5.2.3.1 Hardware The core of the navigator, the industrial PC and the screen, has been selected to develop the navigator. There are numerous solutions on the market for an industrial PC; even the same manufacturers have different solutions depending on the application for which they are intended. Nowadays, many of them also offer low-consumption boards designed for mobile environments.

Three kinds of systems can be distinguished, depending on the level of integration. Completely integrated systems include the PC, screen, and

Figure 5-3 Navigation module for the automotive industry

screen controller. Secondly, systems with the PC and on-board screen controller require an additional separate screen. Finally, basic systems call for the acquisition of the three basic elements—PC, screen, and controller—separately. The advantages and disadvantages of these three systems are summarised in Table 5-1.

SECO's M570 [Seco] (see Figure 5-4), a basic system, is the one that best suits the requirements of the system and offers the best quality for its price. Its versatility, its high number of connectors, and the fact that the manufacturer is able to supply all the components were contributing factors to the selection of this system. Moreover, it is expandable by means of the PC/104-Plus connector.

Additionally, a touchscreen has been added in order to improve the user interface. The user can completely manage the navigator via the screen, selecting maps, searching routes, and so on. A picture of the system in the lab can be seen in Figure 5-5.

5.2.3.2 Industrial PC There can be a number of choices found among the different processors. The processor selected for the module, is the: PC/104 CPU VIA Eden ESP 6000, which offers 600MHz with a PC/104-Plus connector. M570 [Seco] technical characteristics are shown as follows.

- CPU VIA EDEN (ESP4000—400MHz, ESP6000—600MHz, ESP8000—800MHz, ESP10000—1GHz)
- Two 64K L1 cache, one 64K L2 cache
- Bus speed up to 133MHz
- One SODIMM slot
- VIA VT8606 "Twister-T" Northbridge
- VIA VT82C686B Southbridge
- 512KB flash memory BIOS directly soldered on board
- PCI Bus Rev. 2.2, accessible through PC/104-Plus connector

TABLE 5-1 Advantages and disadvantages of industrial PCs

	Advantages	Disadvantages
Completely integrated	Easiest and simplest option	High price Fixed configuration
On-board controller	Moderate freedom with screen	More complex PC-screen compatibility
Basic system	Cheapest solution High freedom Expandable	Bulkier than other systems

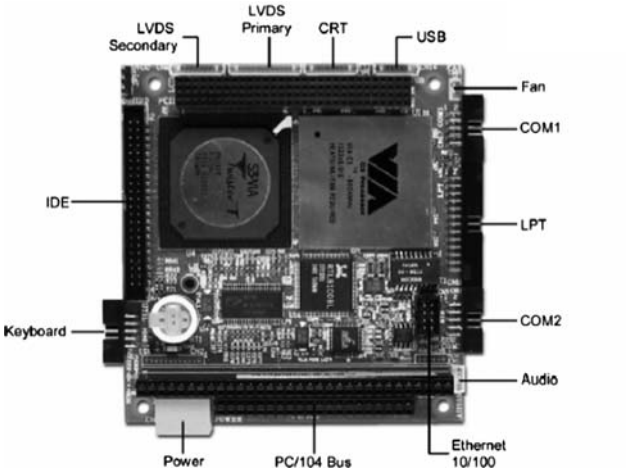

Figure 5-4 M570 of SECO [Seco]

- ISA bus accessible through PC/104 connector
- 2.5-in. HDD UltraDMA-66 or DOM connector
- Ethernet 10/100BaseT interface
- AT keyboard connector
- PS/2 mouse connector
- LPT port configurable in SPP, bidirectional, ECP and EPP mode

Figure 5-5 Entire system at the laboratory

- LPT connector programmable for the connection of an external FDD
- Two serial ports: one full modem RS-232, one programmable as RS-232/RS-422/RS-485
- Dual-channel audio port, 1W per channel
- Two USB 1.1 ports
- Integrated graphic controller
- Resolution up to 1920*1440*64K or 1760*1440*16.8 million colours with CRT monitor
- Dual-channel LVDS interface
- Support for TFT displays with resolution of 640x480, 800x600, 1024x768 or 1280x1024.
- Temperature, fan speed, and voltage monitor
- Power supply required: +5VDC, +12VDC
- PC/104 form factor: 3.5in.×3.8in. (90mm×96mm)

And the parts that the PC module is composed of are:

- CPU (PC/104 CPU VIA Eden)
  - ESP 6000—600MHz, no PC/104-Plus connector
  - ESP 6000—600MHz, with PC/104-Plus connector
  - ESP 10000—1GHz, no PC/104-Plus connector
  - ESP 10000—1GHz, with PC/104-Plus connector
- Memory
  - 128MB SO-DIMM module
  - 128MB IDE flash disk (with WinCE. NET 4.2)
- Display
  - TFT LCD Display 6.5-in. 640/480 300cd/mq 2 CFL
  - Connection cable M570/ML528/Inverter
  - Inverter TDK
  - LVDS receiver module for TFT display 6.4in.
- Touchscreen
  - Resistive touchscreen four wire 6.5in.
  - Interface touchscreen controller for four wire resistive
- Cable kit
  - Connection cable kit

5.2.3.3 Software Navigation software needs to be developed to deal with the information received from the receiver, process that information, and manage both maps and the user interface. The application works with the previously described hardware and processes the data from the GPS receiver and aerial photo maps to provide the user with a visual representation of the location.

5.2.3.3.1 Development Environment Thanks to the Windows CE operating system, many well-known development tools are available. In this case, Microsoft's Embedded Visual C++ 4.0 Tools has been selected. This tool, which differs significantly from any other Windows-based software, is available at Microsoft's webpage. However, the system's numerous limitations must be taken into account. The developing process is briefly described as follows:

1. One of the advantages of having Windows CE on the industrial PC is that programming and checking can be done on a regular PC using an emulator provided by Embedded Visual C++ 4.0 Tools.
2. After the application is developed, the industrial PC can be connected to the PC via serial, USB, or Ethernet. This allows for the debugging of the application on the industrial PC.

Having Windows CE on the navigator is not only useful for the development of the software, but also to improve the module features, which use additional applications. Thus, a multifunctional module has been developed where the user could have, apart from the navigator, multimedia applications such as MP3, video, and DVD players and such in the same module. Moreover, Internet access can be made available by simply adding a 3G module to the system.

5.2.3.3.2 Map Management Due to the large size of maps and the limitation of the system to store and process every map, a map management system has been developed. Maps will be downloaded from a secondary storage system (CD-ROM, pen-drive) as required. When the program starts, it creates a table in the memory, linking every map in order to download the required map every time. This system is totally user-friendly. A screen display of the application is shown in Figure 5-6.

5.2.3.4 User Interface The program is user-friendly and intuitive. Although it is a standard Windows environment with menus and toolbars, it also allows tactile use thanks to the touchscreen. Available options are shown in the following section.

5.2.3.4.1 View Tools The view tools work in the same fashion as conventional image processing software. Basic options are listed as follows:

Figure 5-6 User interface

- Zoom in: This button allows the user to amplify and centre the map at the exact point where the user clicks the mouse. Zoom ratio is defined as 10 percent for every click.
- Zoom out: The same as the previous one, but the image zooms out rather than in. The zoom ratio is also 10 percent.
- Move: This tool allows the map to be moved in eight different directions. Depending on the location of the cursor, its shape will change to one of the directional arrows.

The Coordinates option is also a very useful tool, because it shows the coordinates of the selected point in two different standards (see Figure 5-7).

Moreover, the Monitor button of the toolbar shows the user the location, speed, direction, altitude, time, and number of satellites in view, as well as a magnet displaying the direction of the receiver. The use interface is shown in Figure 5-6.

5.2.3.4.2 Serial Connection The Serial Connection option for the GPS can be found in the Serial Connection toolbar. When the program is started, the GPS receiver will be detected and the connection will start automatically. When it receives the first piece of location-related information,

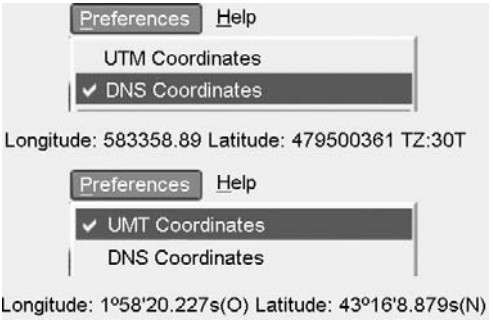

Figure 5-7 Selection of the type of coordinates

the software opens the relevant map containing the user's location. Connection parameters can be set by the users and any changes will be saved in the system register (see Figure 5-8).

A GPS configuration tool is available to correct GPS receiver offset. The actual location and direction can be easily corrected by means of the window shown in Figure 5-9 or by a dynamic capture. By selecting the option dynamic capture and clicking with the cursor on the map, the user sets the actual position. The program then calculates the offset between the location defined by the receiver and the real location set by the user. Calculated data are saved in the program register. Values are positive or negative depending on the direction of the change (south and west are negative).

The settings of this screen are as follows:

- **Position Offset** The offset of the real location is introduced in metres. The software will apply this setting offset to the data received by the receiver.

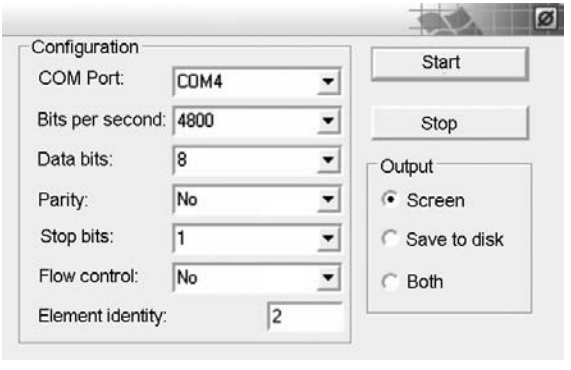

Figure 5-8 GPS serial connection window

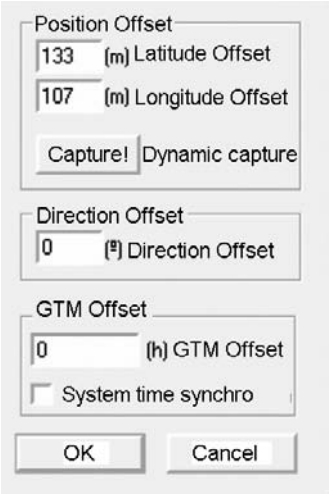

Figure 5-9 GPS configuration window

- **Direction Offset** The direction offset is set in degrees. The 0º reference is north or south increased counterclockwise.
- **GMT Offset** GPS receiver data also provide highly accurate universal time. To set the time, the program must introduce regional time differences.
- **System time synchro** The PC's clock provides the time when the navigation data served by the receiver fail to do so. It is advisable to synchronise the time to avoid the possibility of erroneous data from the software simulation. Moreover, it is a good way to have the PC's clock synchronised to a reliable source such as the GPS.

5.3 Summary

In this chapter a number of different fields which will be of benefit to a dual GPS/Galileo receiver have been listed and described. Moreover, the development of an entire receiver car module: selection of the digital processing receiver, onboard PC, touchscreen and software development has been described.

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Chapter

6

Conclusions

The main objective of this book is to show how to design, fabricate, and test a highly integrated, low-noise, low-power, and low-cost radio frequency (RF) front-end, focusing on the Global Navigation Satellite System (GNSS) standards GPS and Galileo. Starting from the very beginning, this book spans the entire process, ultimately providing you with everything necessary for a market-ready receiver. To guide this process, we have defined and described a number of objectives throughout the book.

The viability of GPS and Galileo's interoperability has been shown. It has been demonstrated that a receiver can handle both standards simultaneously. Secondly, RF front-end requirements regarding gain, noise, bandwidth, and rejection of interferences have been set to be compatible with both systems. The specifications of the blocks of the front-end have been obtained by means of analysis simulation and a study of state-of-the-art blocks.

Although simulations provide acurate estimations of the RF front-end performance, previous to the mass fabrication, a validation stage is required. To validate the design, designers must fabricate the RF front-end. However, a technology must first be chosen before design begins. The AMS HBT 0.35μm SiGe process has been selected for the design example. The viability of an RF application such as that proposed in this book has been proved. Moreover, among all the existing architectures for an RF front-end, the intermediate frequency (IF) has been selected and its suitability for a GPS and Galileo RF front-end has also been demonstrated. This relatively simple architecture is easy to integrate, and its main disadvantage can be overcome by means of a good frequency plan, that is, image signal rejection can be achieved. Moreover, this architecture is suited for the three proposed structures

that allow the use of the front-end for different applications, depending on power consumption and the antenna, which gives the end user a high level of versatility.

Every component of the front-end has been selected, and the architecture, design, and layout of each have been successfully carried out by applying a number of techniques explained in this book. This has also been reflected in the experimental results. The performance of every block of the RF front-end of the design example can be compared to that of state-of-the-art components.

Of the front-end components proposed in the design example, three in particular should be pointed out. The dual-gain low-noise amplifier (LNA) allows the use of the proposed structures and automatically detects the presence of an active antenna, switching on the gain mode. The joined RF amplifier and mixer design have increased the gain current consumption ratio with a low noise figure. In addition, a highly integrated phased-lock loop (PLL) has been designed with a two output frequency selection, which minimises the need for external components. These are the main components necessary to achieve a low-power, low-noise, and highly-integrated RF front-end.

The floor-planning of the front-end allows the most critical components to be isolated from each other considerably without compromising the information signal, by properly placing them within the integrated circuit (IC). To protect it from electrostatic discharges (ESD) produced during handling, ESD protections have also been included. Additionally, the designed control logic allows four operation modes for the front-end: on, off, having only the digital part switched on for the clock signal/digital processor, and test mode. The last mode allows the testability of the front-end and, together with the intermediate pads added, enables the different blocks of the front-end to be measured separately. This allows the designer to save considerable money and time due to faster and cheaper market availability, since the front-end blocks do not have to be fabricated and validated separately. However, the passive components have been characterised and modelled previously on-wafer separately from the entire IC, achieving the required performance for the final design.

Finally, designs of the printed circuit board (PCB) for IC characterisation, as well as the selection of required external components, have been carried out, making the validation of the entire prototype possible.

At this point, the design of the GPS/Galileo front-end has been successfully completed. Every step of the design, from standards analysis to characterisation, has been explained in this book. The performance of the RF front-end is summarised in Table 6-1.

The performance of the receiver can be compared to state-of-the-art devices presented in scientific papers as well as commercial ones.

TABLE 6-1 RF front-end measured results

Process	0.35μm SiGe
Current consumption	23mA
Front-end bandwidth	6MHz
Voltage gain	103dB
Noise figure	3.7dB
LO phase noise @ 100kHz	–84dBc/Hz
Front-end size	2.8×3.0mm2

Table 6-2 compares the best state-of-the-art front-ends, shown in Chapter 1, with the design example of this book in terms of gain, noise figure (NF), and current consumption.

As shown in Figures 6-1 to 6-3, the design example of this book does not improve any of the three parameters when considered separately. However, without compromising any of these three parameters separately, it is one of the best designs when it comes to having these three parameters together. Therefore, it achieves a good performance in terms of gain, noise, and current consumption, which makes it suitable for any high-accuracy, portable application.

In addition to the enhanced performance of the front-end, the design takes advantage of the interoperability of GPS and Galileo. As reflected

TABLE 6-2 Comparison of the proposed RF front-end to state-of-the-art devices

Reference	Gain [dB]	NF [dB]	Current Consumption [mA]
[Shaeffer98]	98	4.1	37
[Cloutier99]	120	4	16
[Kadoyama04]	110	4	15
[Chen05]	27.7	4.13	12
[Sahu05]	38	2	43
[Freescale MRFIC1505]	105	2	28
[MAXIM MAX2769]	96	1.4	18
[PHILIPS UAA1570HL]	148	4.5	55
[SiGe SE4120L]	18	>1.6	10
[ST STB5610]	139	3	40
Design example	103	3.7	23

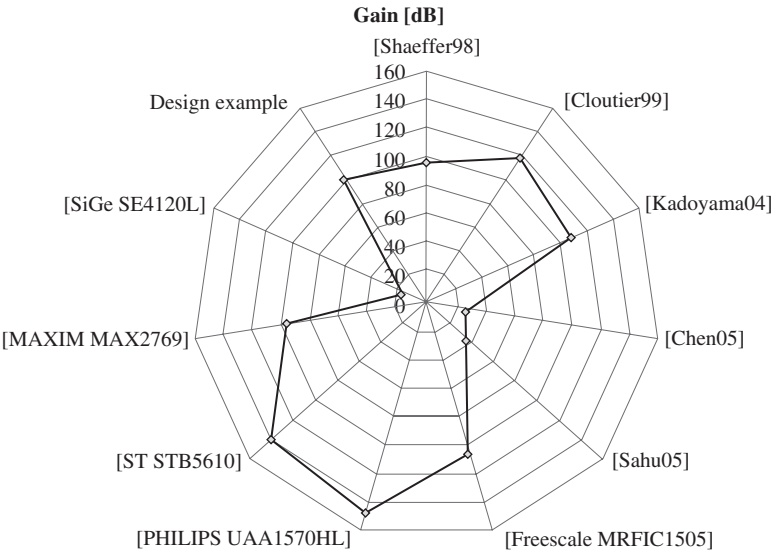

Figure 6-1 Gain comparison for the design example and state-of-the-art devices

in Chapter 1, there are very few references to GPS/Galileo dual front-ends at present. This fact will change in the near future due to the numerous advantages of a dual receiver, as shown in the opening chapters of this book.

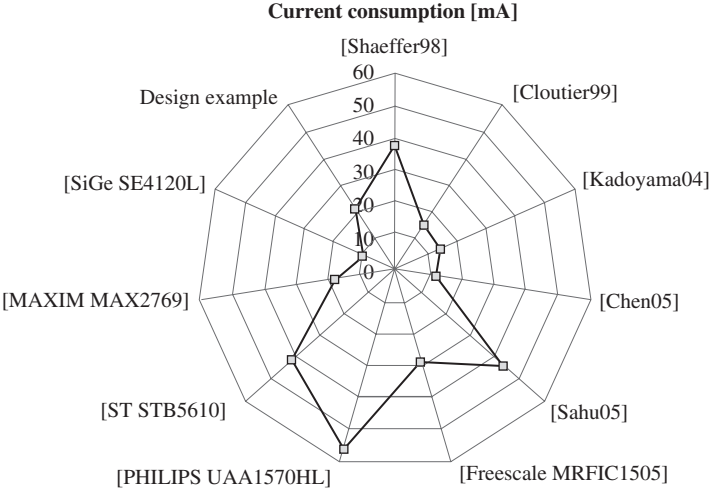

Figure 6-2 NF comparison for the design example and state-of-the-art devices

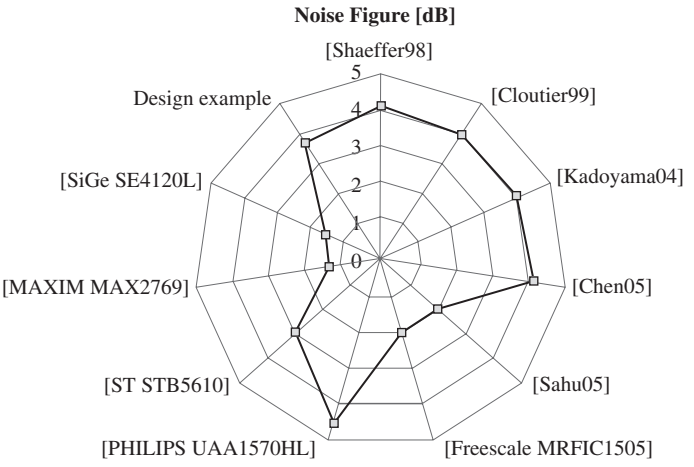

Figure 6-3 Current consumption comparison for the design example and state-of-the-art devices

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